Bi-directional Flyback DC-DC Converter for Battery System of the DC House Project

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ABSTRACT

BI-DIRECTIONAL FLYBACK DC-DC CONVERTER FOR BATTERY SYSTEM OF DC HOUSE PROJECT

Austin Luan

The DC House project strongly relies on renewable energy sources to provide power to the house for various loads. However, when these sources are unable to provide power at a certain time, a back-up energy source from a battery must be readily available to fulfill the house's power needs. This thesis proposes a bi-directional flyback power converter to allow a single-stage power path to charge the battery from and to discharge the battery to the DC House 48 V system bus. The design, simulation, and hardware prototype of the proposed flyback bidirectional converter will be conducted to demonstrate its feasibility. Results from a 35W prototype demonstrate the operation of the proposed converter for both charging and discharging purposes.

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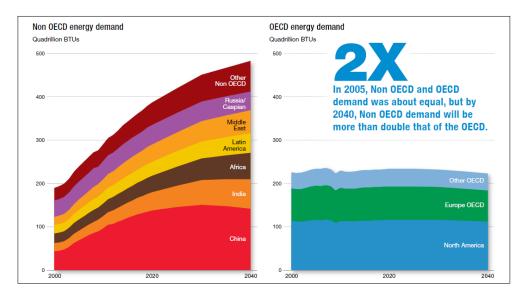
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Chapter 1 – Introduction

1.1 The Demand for Energy

According to the Census Bureau, the world population has steadily increased from 2,557,628,654 people in 1950 to 7,095,217,980 in 2013 [1]. Because of increasing population in the world, energy demand in developing nations is expected to rise 65 percent by 2040 compared to 2010, reflecting growing prosperity and expanding economies [2]. In response to the population growth, a greater demand for electricity will be seen from all developed and rural countries [2]. Figure 1-1 reflects the projected energy demand from 2010 to 2040 for different continents and countries.





For the next 30 years, electricity generation represents the largest energy use across four different sectors: industrial, transportation, electricity generation, and residential/commercial. However even with advancements in science and technology, according to the International Energy Agency (IEA), around 1.3 billion people today still do not have access to electricity [2]. Therefore, in order to help combat the dependency on electricity, renewable energy has become a larger priority in order to help provide for those that do not have electricity especially in areas inaccessible by the utility grid. According to the US Energy Information Association, renewable energy accounts for 32 percent of the overall growth in electricity generation from 2011 to 2040 [3]. The ability to provide electricity power through both new methods and renewable energy creates an opportunity for new technology to meet the electricity demand such as the DC House Project.

1.2 The DC House Project

The DC House project is an open source project initiated by California Polytechnic State University consisting of master theses and senior projects in hopes of creating an operating house whose electricity is provided from DC power. The purpose of the DC House project is to help those in third-world countries receive electricity in locations that are not accessible to grid generation. In our predominately AC system, small-scale renewable energy sources are generally putting out DC power and hence require intermediate energy conversion to AC in order to be accessible to the consumer [4]. However, converting from DC power to AC power may imply extra cost for equipment to implement such a system as well as potentially increase the amount of power loss that the system experiences and thus reducing the overall efficiency of the system. The DC House attempts to bypass such a power conversion in order to provide enough energy for typical household items without the reliance of AC power.

The DC House project has been broken into three separate phases. Phase 1, which was completed at the end of 2011, focused on the initial study and modeling of individual DC powered home including the design for several possible DC power sources [5]. These possible sources include a hydro-power generator [6], a photo-voltaic generation system, a wind power generator [7], and a bicycle powered generator [8]. Besides the inclusion of different DC power

2

sources, Phase 1 also included the preliminary design of the multiple-input-single-output (MISO) DC-DC converter that ties all the outputs of the possible DC energy sources to a single output which provides the main DC bus voltage that feeds power to the DC house [9].

Phase 2, which was completed at the end of the 2012, emphasized on a DC distribution system and protection and a human-powered generator [10]. A DC House model was built at Cal Poly as a prototype to be used for the DC House project. Phase 2 also introduced multiple senior projects and theses to develop the interface of the DC house to DC loads such as a dimmable DC light bulb [11], a cell phone charger, and a smart variable voltage DC wall outlet.

Phase 3, which is to be completed by 2013, attempts to improve the MISO converter as well as a generator model. Other applications such as a bi-directional battery charger, a removable DC light bulb, a low speed generator, and more human-powered generators are being developed. Figure 1-2 shows the block diagram of the DC house with the renewable sources in the front end and the various load applications in the DC house [4].

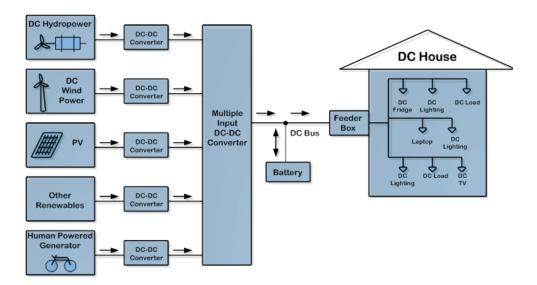


Figure 1-2: DC House Block Diagram [4]

Chapter 2 – Background

2.1. Lead-Acid Batteries

The most common rechargeable battery that is commonly used on a daily basis is leadacid batteries because of their robust capacity to provide power and higher nominal voltages per cell compared to other secondary batteries. Lead-acid batteries have a low energy-to-weight ratio as well as low energy-to-volume ratio which enable them to supply high surge currents while allowing the cells to maintain a large power-to-weight ratio. Because of these features, lead-acid batteries are used most exclusively for motor vehicles to provide high current for automobile starter motors [17].

Lead acid batteries are divided into two different types: starting lead-acid batteries and deep cycle batteries. The starting battery is designed to deliver quick bursts of energy (such as starting engines) and therefore has a greater plate count. The plates are thinner and have somewhat different material composition [20]. The deep cycle battery has less instant energy, but greater long-term energy delivery. Deep cycle batteries have thicker plates and can survive a number of discharge cycles [20]. Starting batteries should not be used for deep cycle applications because the thinner plates are more prone to warping and pitting when discharged.

Figure 2-3 shows the interior of a deep cycle lead acid battery. Typically a lead-acid car battery consists of 6 individual cells that are used to for electrochemical reactions to produce electricity and power. Each individual cell's voltage can range between 2.15V up to 1.85V. For a fully charged car battery, the nominal output voltage is around 13V while a fully discharged car battery has a nominal output voltage of 11V [20].

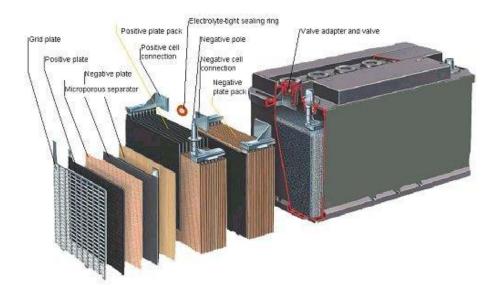


Figure 2-1: Interior of a Deep Cycle Lead Acid Battery [14]

There are two general rules of thumb to determine the amp hour ratings of a lead-acid car battery based upon the reserve capacity (RC). The reserve capacity of a battery is defined as the number of minutes a fully charged battery at 80 ° F will discharge 25 amps until the battery drops below 10.5 volts [18]. Using the reserve capacity of a battery, the amp hours rating can be determined by either multiplying the RC value by 0.6 or dividing the RC value by 2 and adding 16 to that resultant value [19].

2.2. Bi-directional Power Flow

A majority of DC-DC converters provide current in a unidirectional fashion by having a single path for current to flow from the input source to the load. For example, a non-isolated topology known as the Buck converter provides current from the input source to the output through the MOSFET switch, the inductor, and the free-wheeling diode during the time when the MOSFET switch is off. Because of the inability for the switch and the diode to carry current in the reverse direction from the load to the input voltage source, the Buck converter is a unidirectional DC-DC converter.

Bi-directional DC-DC converters fall into a generic circuit structure illustrated in Figure

2-4 which is characterized by current or voltage being fed from one side to the other [16]. Based upon the magnitude of the voltage and current as well as the placement of the energy storage items, the bi-directional DC-DC converter can either operate as a Buck converter by stepping down a higher voltage to a lower voltage or as a Boost converter by stepping up from a lower voltage to a higher voltage.

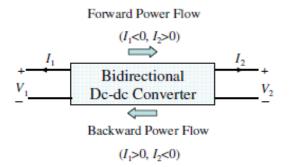


Figure 2-2: Generic Circuit describing Power Flow of a Bi-directional DC-DC Converter [16]

In order to allow bi-directional power flow between two energy storage items with a DC-DC converter, a secondary switch and a reverse diode on the main commutating switch is needed for a uni-directional converter. Figures 2-5 and 2-6 illustrate that implementation with an additional switch added upon the secondary diode and a reverse diode augmented on the main switch to allow two paths for current flow.

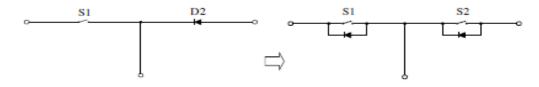


Figure 2-3: Addition of Secondary Switch and Reverse Diode for Bi-directional Power Flow [16]

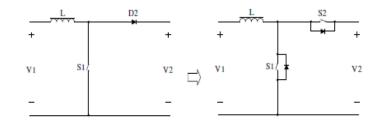


Figure 2-4: Addition of Secondary Switch and Reverse Diode for Bi-directional Power Flow (Boost Example) [16]

Bi-directional DC-DC converters have been used in applications for charging batteries, electrical vehicle motor drives, and interruptible power supplies. Such topologies that have been used include a non-isolated topology such as the buck-boost and isolated topologies such as the half-bridge, the full-bridge and the flyback. The non-isolated buck-boost is an advantageous topology because the converter does not require the transformer to be used as an energy transfer or energy storage component and for applications that do not require isolation between the input and output [21]. Despite the lack of a transformer, the buck-boost topology relies heavily on soft switching techniques such as zero voltage switching (ZVS) or zero current switching (ZCS) in order to compensate for high voltage spikes seen by switching MOSFETs and inductors [21]. The half-bridge and full-bridge topology are suitable for high power applications and high voltage applications but require large amounts of components and use of snubbers, making the design portion of the converter complex [22]. The flyback topology on the other hand uses the transformer as an energy storage device, but the topology yields low costs, good transient response, and low amount of components [23].

As long as the requirement of allowing two paths of current flow is satisfied, any topology, non-isolated or isolated, can be converted into a bi-directional topology. Because of the low amount of required components, the use of the transformer to compensate for low duty cycle, and the availability of controller chips for commercial purchase, the flyback topology will be chosen for the proposed bi-directional DC-DC converter. The objective of this thesis is therefore to investigate the use of the flyback topology for the bi-directional DC-DC power converter. The bi-directional power converter is needed for the battery system used in the DC House project. The design, simulation, and hardware prototype of the proposed flyback bidirectional converter will be conducted to demonstrate its feasibility. Results from simulation and hardware implementation will be presented in this report as well as lessons learned and further recommendations to improve the design.

Chapter 3 – Design Requirements

3.1. Battery Configuration

As stated in the previous chapter, the objective of this thesis is to design and build a bidirectional DC-DC converter for the battery system in the DC house project. As stated in Chapter 1, the lead-acid battery is a suitable back-up power source to model the bi-directional DC-DC converter because of its charging capacity as well as the battery's robust ability to provide power through chemical reactions. In order to properly size the bi-directional converter, a proper leadacid battery configuration must be determined.

Two different configurations will be considered when arranging the batteries: batteries connected in series or batteries connected in parallel. Connecting batteries in series can increase the overall voltage of the composition but the amp hour rating stays the same [24]. This is beneficial in terms of allowing a higher duty cycle for the DC-DC converter based upon the input voltage of the bi-directional converter and the terminal voltage of the battery configuration. Connecting the batteries in parallel would increase the overall amp hour rating of the configuration, but the voltage remains constant with the terminal voltage of a single battery [24]. Connecting the batteries in parallel would require the use of small resistors connected in series with the batteries to prevent the current from cycling within the same loop between two batteries in parallel. Figure 3-1 gives an example of how voltage and amp ratings for batteries change based upon the configuration of the battery.

Series Connection

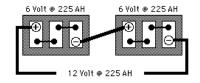


Figure 3-1: Voltage and Amp Ratings based upon Battery Configuration [24]

However, connecting batteries in either configuration would require that the settings and characteristics of each battery to be identical in order to operate in ideal conditions. Because the bi-directional DC-DC converter will be used for accessible used car batteries, it is strongly discouraged to use such configurations for safety purposes. Thus, the battery set-up for the bi-directional battery charger will be a single lead-acid car battery.

Using the battery configuration choice, output voltage, input voltage and output current for one side of the bi-directional converter can be determined. As stated in Chapter 2, a fully charged lead-acid battery has a nominal voltage of close to 13V while a completely discharged lead-acid battery has a voltage of 11V. These two voltage values will be used as the maximum and minimum input voltage respectively for when the battery is discharging power to the DC House. The 12.5V will be used as the output voltage in which the lead-acid battery will be charged upon. A higher voltage of 12.5V is chosen instead of 12V in order to compensate for any switching or leakage losses from the converter. Because the output voltage will be held at 12V, the lead-acid battery will be charged using a constant current method. Lead-acid batteries have two different methods for current charging: fast charge or slow charge [24]. A fast charge current uses 6A or higher to quickly charge the car battery. For safety reasons, the maximum fast charge current is typically rated at 10A. A slow charge current uses 2A to charge the car battery. A disadvantage for using a slow charge current compared to a fast charge current is the charging time for a lead-acid battery. However, in order to preserve the battery to as long as possible while being sustainable, a slow charge current will be used instead. Thus, the output current for when the bi-directional converter is charging the battery will be 2A. With the output voltage and output current determined based upon the battery configuration, the output power for the charging stage of the bi-directional converter will be 24W.

The DC House has an established 48V bus line that is directly connected between the front-end generation and the DC House feeder. The bi-directional converter will be connected in between generation and the DC House. Thus, the input voltage for the charging stage of the bi-directional converter and the output voltage for the discharging stage converter will be 48V. The output power for the discharging stage can be determined by the ampere-ratings of the battery and the magnitude of the discharging current. Table 3-1 shows preliminary calculations for discharge current and output power for different lead-acid car batteries based upon their ampereratings. As stated in Chapter 2, the ampere-ratings of a lead-acid battery can be determined by dividing the reserve capacity by 2 with an addition of 16.

		For 96 Ah	For 70 Ah
Output Power (W)	Current From DC	Time to Discharge	Time to Discharge
	House Load (A)	(Hours)	(Hours)
500	10.42	9.22	6.72
450	9.38	10.24	7.47
400	8.33	11.52	8.40
350	7.29	13.17	9.60
300	6.25	15.36	11.20
250	5.21	18.43	13.44
200	4.17	23.04	16.80
150	3.13	30.72	22.40
100	2.08	46.08	33.60

 Table 3-1: Preliminary Calculations of Discharge Time based upon Output Power and Lead-Acid Battery Ampere-Rating

Based upon the preliminary calculations shown in Table 3-1, the output power will be chosen based upon the "worst-case" scenario of the two amp-rated batteries and the discharging time requirement of more than 10 hours. With these two considerations, the output power for the discharging stage of the converter will be 300W. With an output voltage of 48V, the output current for the discharging stage of the converter will be 6.25A.

3.2. Topology Selection

As stated in Chapter 2, any uni-directional converter can be turned into a bi-directional converter by adding an additional secondary switch on the output diode and a reverse diode on the main commutating switch. Due to its lower cost, low component count, good transient response, and the ability to use the turns ratio to increase the duty cycle of the overall system, the flyback topology will be used for the proposed DC House bi-directional converter [24]. Two different flybacks will be chosen to regulate the discharging and charging stages of the bi-directional converter. Figure 3-2 shows the power stage of the dual flyback with the reverse diodes placed across the switches to make the converter bi-directional. Two controller chips will be selected based upon the output voltage and power requirements defined in this chapter.

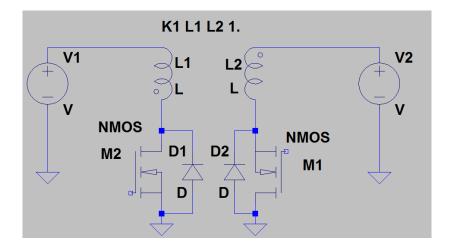


Figure 3-2: Dual Flyback Power Stage of Bi-directional Converter

3.3. Design Requirements Overview

Efficiency is an important aspect of the bi-directional converter because of the lifetime of the car battery as well as reducing the amount of switching losses from two separate flyback topologies. Therefore, the proposed design is expected to operate with greater than 80% efficiency at maximum load for both the charging and discharging stage. Although the integrity of the output voltage is not necessarily important since the battery will be charged using constant current, the output voltage ripple will be expected to be less than 5% of the 48V output for the discharging stage and the 12.5V output for the charging stage. Line and load regulations will be less than 5% for both the discharging and charging stage of the bi-directional DC-DC converter.

In order to preserve the lifetime of the battery, the maximum output power for the discharging stage is ideally 150W to reduce a fast discharge from the battery. However, because this thesis is a proof of concept of the bi-directional configuration, the discharging flyback output power will be designed to be 48W. The maximum output power stage for the charging stage is selected to be 24W because an output current of 2A is a slow charge current for the battery. Table 3-2 summarizes the design requirements for the proposed bi-directional converter.

	Charging Stage	Discharging Stage
Input Voltage	$48V\pm5\%$	(11V-13V), 12V Nominal
Output Voltage	12.5V	48V
Maximum Output Current	2A	1A
Maximum Output Wattage	25W	48W
Line Regulation	5%	5%
Load Regulation	5%	5%
Output Voltage Ripple	5%	5%
Efficiency at Full Load	≥ 80%	≥ 80%

Table 3-2: Specifications of the Bi-directional DC-DC Converter

Chapter 4 - Design and Simulation Results

In this chapter, the proposed bi-directional converter design to meet the design requirements stated in Chapter 3 will be described in detail. The bi-directional converter is broken down into two separate flyback topologies; one for the charging stage from the DC bus line of the DC house of 48V to the battery terminal voltage of 12V, and the other one for the discharging stage from the battery terminal voltage of 12V to the DC bus line of the DC house of 48V. Component calculations, component selection, simulations, and integration of both flyback topologies with a suitable control scheme will be presented in this chapter. A section of this chapter will also detail the custom flyback transformer design for the bi-directional converter.

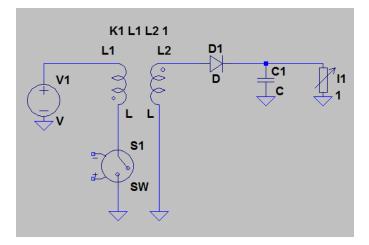


Figure 4-1: Basic Flyback Schematic

As stated in Chapter 3, the advantages of using a flyback topology include low component count, good transient response, low circuit costs, and the use of the transformer as an energy storage component rather than an energy transferring device with the use of its magnetizing inductance. The flyback also does not require the use of an output filter inductor or a free-wheeling diode, as shown in Figure 4-1, which reduces the complexity of the circuit. Compared to other topologies used for bi-directional power flow, the flyback offers a larger profile of controller chips that can be easily controlled compared to the controller chips for the buck boost, full-bridge, and half-bridge topologies.

When the switch is on, the input voltage source provides current that flows through the primary winding of the transformer and the switch. Energy is being stored in the magnetizing inductance of the transformer at a rate of the input voltage over the magnetizing inductance. However, there is no current flowing in the windings of the transformer. At the same time when energy is being stored in the magnetizing inductance of the transformer, the load current is being supplied from the output capacitor. The output diode is reversed biased, making an open during the time the switch is on.

When the switch is off, the energy stored in the magnetizing inductance is released through the secondary winding of the transformer. The release of energy forces the output diode to conduct and allows energy to transfer to the load after being filtered by the output capacitor.

4.1. Flyback Design for Charging Stage

Based upon the design specifications listed in Chapter 3, the maximum output power seen by the charging stage of the bi-directional converter will be 24W. Because of the power constraint, the LT3748 controller chip is chosen because of its power rating as well as its ability to derive information from the output voltage based upon the primary-side flyback pulse waveform [27]. The maximum output power for the controller is limited due to the external components of the IC. The output power limitations are separated into three categories – voltage limitations, current limitations, and thermal limitations [27].

The controller features a boundary mode control method, where the controller operates between continuous conduction mode and discontinuous conduction mode. With boundary control mode operation, the output voltage can be derived from the transformer primary voltage

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when the secondary current is almost zero. Using this feature reduces the size of transformer, excludes subharmonic oscillations, and improves load regulation [27]. Figure 4-2 shows a block diagram of the LT3748 and functionality.

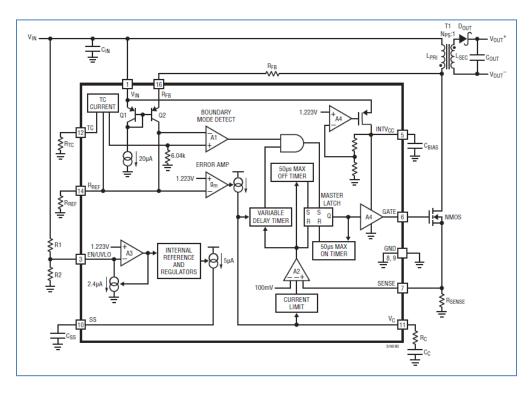


Figure 4-2: LT3748 Block Diagram [27]

The duty cycle of the flyback can be determined using the following equation given from the LT3748 datasheet [27]:

$$D = \frac{(V_{out} + V_F(diode)) * N_{PS}}{V_{in} + (V_{out} + V_F(diode)) * N_{PS}}$$
(4.1)

where N_{PS} is the turns ratio N_p/N_s , $V_{F (diode)}$ is the forward voltage drop across the output diode, V_{in} is the input voltage of the flyback, and V_{out} is the output voltage of the flyback. Assuming a forward voltage drop of 1V, input voltage of 48V, a turns ratio of 4, and an output voltage of 12.5V, the nominal duty cycle is approximately 52%.

The LT3748 uses a sense resistor to optimize the current limit of the primary side current. Using the following equations given by the datasheet [27]:

$$R_{sense} = \frac{100 \, mV}{I_{Lmin}} \tag{4.2}$$

$$I_{Lmin} = I_{o(max)} * \frac{2}{N_{PS} * 0.85 * (1-D)}$$
(4.3)

where I_{Lmin} is the minimum peak inductance current on the primary side of the transformer. The minimum primary side peak current can be determined using Equation 4.3 from the maximum output current $I_{o(max)}$, the turns ratio N_{PS} , and the duty cycle D. With a maximum output current of 2A, a turns ratio of 4, and a maximum duty cycle of 0.52, the minimum primary peak inductance current was determined to be 2.45A.

For headroom purposes, the primary inductance peak current used to determine the R_{sense} value is rounded up to 3A. Assuming an I_{Lmin} value of 3A, the R_{sense} value was determined to be 33m Ω . A 100 Ω resistor will be connected in series from the SENSE pin to the sense resistor with a 10000pF capacitor connected in parallel across the sense resistor to provide a cutoff frequency of 160 kHz to reduce noise interference from other components.

A proper transformer must be selected in order for the flyback current requirements to be met. For the purpose of designing the charging flyback, a turns ratio and minimum primary inductance value will be determined. A more detailed design approach for the transformer will be described later on in this chapter. The turns ratio for the transformer was determined to be 4:1 based upon the input voltage (48V) and the output voltage (12.5V).

Because LT3748 obtains its output voltage information from the external MOSFET drain voltage when the secondary winding conducts current, the sampling circuitry requires a minimum of 300ns to settle and sample the output voltage while the MOSFET switch is off [27]. This required settle and sample time is controlled by external components independent of the minimum off-time of the GATE pin. Therefore, the primary inductance must satisfy the following equation obtained from the datasheet:

$$L_{PRI} \ge \frac{(V_{out} + V_{F(diode)}) * R_{sense} * N * t_{settle(min)}}{V_{sense(min)}}$$
(4.4)

where N is the turns ratio of the transformer, V_{out} is the output voltage, $V_{F(diode)}$ is the forward voltage drop of the output diode, $t_{settle (min)}$ is the settle time for the controller, and $V_{sense (min)}$ is the minimum voltage for the sense pin. Assuming a forward voltage drop of 1V, output voltage of 12.5V, a turns ratio of 4, a sense resistor of $33m\Omega$, a settle time of 400ns, and a minimum sense voltage of 15mV, the minimum primary inductance must be greater than 45.8 uH.

Besides the primary inductance requirement for minimum settling and sampling time, the LT3748 has internal circuit constraints that prevent it from setting the GATE node high for shorter than approximately 250 ns [27]. The primary inductance must also satisfy the following equation obtained from the datasheet:

$$L_{PRI} \ge \frac{V_{in\,(\text{max})*R_{sense}*t_{on(\text{min})}}}{V_{sense\,(\text{min})}}$$
(4.5)

where $V_{in(max)}$ is the maximum input voltage, R_{sense} is the sense resistor of the SENSE pin, V_{sense} (min) is the minimum sense voltage for the SENSE pin, and $t_{on (min)}$ is the minimum on time of the GATE pin. Assuming a maximum input voltage of 50V, a sense resistor of 33m Ω , a suggested minimum on time of 250ns, and a minimum sense voltage of 15mV, the minimum primary inductance for preventing the setting of the GATE node to be high for shorter than 250ns must be greater than 27.5 uH.

The final constraint on the minimum inductance is related to the full-load operating frequency, f_{min} [27]. The final constraint for the primary inductance value must satisfy the following equation obtained from the datasheet:

$$L_{PRI} \le \frac{V_{in\,(\text{min})}*N_{PS}*(V_{out}+V_{F\,(diode)})}{f_{SW\,(\text{min})}*I_{Lmin}*(N_{PS}*(V_{out}+V_{F\,(diode)})+V_{in\,(\text{min})}}$$
(4.6)

where $V_{in \text{ (min}}$ is the minimum input voltage, N_{PS} is the turns ratio of the transformer, V_{out} is the output voltage, $V_{F \text{ (diode)}}$ is the forward voltage drop across the output diode, $f_{SW \text{ (min)}}$ is the minimum switching frequency at maximum load, and I_{Lmin} is the minimum primary inductance current. Therefore, assuming a minimum input voltage of 48V, a turns ratio of 4, an output voltage of 12.5V, a forward diode voltage drop of 1V, a minimum switching frequency of 42 kHz from the datasheet, and a minimum primary inductance current of 3A, the primary inductance related to full-load operating frequency must not be greater than 82.5 uH. With these three constraints on the primary inductance, the appropriate value chosen was 70 uH. Using the turns ratio, the secondary inductance of the transformer is chosen to be 4.375 uH.

The output diode and MOSFET must be properly sized based upon the following two equations given in the datasheet [27]. The theoretical maximum drain-source voltage is given in Equation 4.6 while the theoretical maximum output diode reverse voltage is given in Equation 4.7:

$$V_{DS(\max)} = V_{in(\max)} + V_{out(\max)} * N_{PS}$$
(4.7)

$$V_{RRM} = V_{out(\max)} + \left(\frac{V_{in(max)}}{N_{PS}}\right)$$
(4.8)

Assuming a maximum input voltage of 48V, a maximum output voltage of 13V, and a turns ratio of 4, the theoretical maximum drain-source voltage is 96V and the theoretical maximum output diode reverse voltage is 24V. In order to maximize the efficiency of the flyback, the MOSFET chosen must be within the rated drain-source voltage but with minimal $R_{DS(on)}$, and the output diode must be within the rated maximum output diode reverse voltage but with a minimal forward diode voltage drop. Based upon these calculations as well as the minimum primary inductance current of 3A, the charging flyback will be implementing a Vishay Si4490DY NMOSFET rated at 250 V_{DS} with a 4A continuous drain current rating. The output diode will be a LQA30T300 Schottky output diode rated at 300V. Leakage inductance and voltage spikes were taken into consideration when selecting the output diode and the MOSFET switch. For simulation purposes, a MBRB2545CT Schottky diode is used to substitute the LQA30T300 Schottky diode.

Properly sizing the output capacitor is critical to the output voltage peak to peak ripple. Based upon the specifications stated in Chapter 3, the minimum output capacitance value can be calculated based upon the following equation [28]:

$$C_{min} = \frac{D}{R_{min} * f_{min} * \frac{\Delta V}{V_o}}$$
(4.9)

where D is the duty cycle of the flyback, R_{min} is the resistance with full load current, f_{min} is the minimum frequency at worst case scenario, and $\Delta V/V_o$ is the peak to peak ripple. Using a duty cycle of 52%, an R_{min} of 15.36 Ω , a worst case switching frequency of 42 kHz [27], and a peak to peak ripple of 5%, the minimum capacitance required is calculated to be 16.1 uF. For the purpose of the charging flyback, three 10uF X7R capacitors will be connected in parallel with a rated voltage of 50V, creating an overall output capacitance of 30uF. Connecting the capacitors in parallel will reduce the ESR of the output capacitance which helps the overall efficiency of the charging flyback.

The LT3748 derives the output voltage by a resistor ratio between the feedback resistor on the primary side of the transformer and a reference resistor [27]. The reference resistor, ranging from $5.76k\Omega$ to $6.34k\Omega$, is suggested to be nominally set at $6.04k\Omega$. Using the following equation obtained from the datasheet, the feedback resistor (R_{FB}) is determined to be [27]:

$$R_{FB} = \frac{V_{out}}{V_{BG}} * N_{PS} * R_{REF}$$

$$\tag{4.10}$$

where V_{out} is the output voltage, N_{PS} is the turns ratio, R_{REF} is the reference resistor, and V_{BG} is the bandgap voltage of 1.223V that is the reference voltage of the error amplifier within the

controller. With an output voltage of 12.5V, a reference resistor of $6.04k\Omega$, and a turns ratio of 4, the feedback resistor is calculated to be $249k\Omega$.

The LT3748 also allows an enable/undervoltage lockout feature to protect the circuit if the input voltage is under the minimum input voltage of the controller. A resistive divider is formed from the input voltage line to the EN/UVLO pin to create a reference voltage that is compared to the pin threshold voltage of 1.223V [27]. If the reference voltage from the resistive divider is greater than or equal to the threshold voltage, the EN/UVLO will allow the controller chip to operate. Using the following equations obtained from the datasheet, the resistive divider is determined to be:

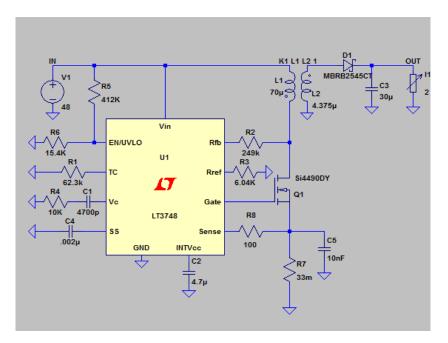
$$1.223V = 48V * \left(\frac{R_2}{R_1 + R_2}\right) \tag{4.11}$$

The resistive value for R_1 was determined to be $412k\Omega$ and the resistive value for R_2 was determined to be $15.4k\Omega$. The ENABLE/UVLO pin is important for the control scheme of bidirectional power flow, which will be described in detail later in this chapter.

The LT3748 uses an external resistor-capacitor network to compensate for the loop gain [27]. Typical values suggested by the datasheet are in the range of $R_C = 50k\Omega$ and $C_C = 1nF$. If the resistor value for R_C is too large, the transient performance is most susceptible to high frequency noise and jitter. If too small, the transient performance will suffer as well. The value choice for C_C is the inverse of the value choice for R_C : if too small of a value, the loop may be unstable and if too large of a value, the transient performance will suffer. Based upon these guidelines, a suitable 10k Ω resistor and 4.7 nF capacitor was chosen for loop compensation.

The $INTV_{cc}$ pin is the input voltage pin that powers the internal circuitry of the LT3748. Based upon the suggested configurations given in the LT3748 datasheet, a capacitor will be connected in series to ground because an external power supply will be used to provide power to the entire circuit. Connected to a capacitor in series with the $INTV_{cc}$ pin will provide a more efficient source of power for internal circuitry and reduce power dissipation in the LT3748 chip [27].

Figure 4-3 shows the complete 48V to 12V charging flyback with calculated resistors and capacitors for each pin of the controller chip. It is important to note that the soft-start pin and output voltage temperature compensation pins are used in this configuration in order to optimize the performance of the charging flyback. Because the soft-start and output voltage temperature compensation are extra features of the controller that are not necessary for charging, calculations and design options were not detailed in this chapter.





4.2. Flyback Design Simulation Results for Charging Stage

Figure 4-4 details the output voltage ripple of the charging flyback with a full load of 2A. The average voltage is determined to be 12.6V, with a peak to peak ripple voltage of 0.4V or 3% of the output voltage. Figure 4-5 shows the voltage of the current sense pin of the LT3748 controller when the charging flyback is supplying power for full load. Boundary conduction mode can be seen as the voltage of the current sense pin drops to zero. Since the voltage of the current sense pin is below the threshold voltage of 100 mV, the MOSFET is able to be turned on and off in order to achieve the output voltage desired.

The line regulation of the charging flyback is determined using Equation 4.12:

$$Line Regulation = \frac{V_{o(high-input)} - V_{o(low-input)}}{V_{o(nom input)}} = \frac{12.6V - 12.6V}{12.5V} * 100 = 0\%$$
(4.12)

The load regulation of the charging flyback is determined using Equation 4.13:

Load Regulation =
$$\frac{V_{o(\min load)} - V_{o(\max load)}}{V_{o(\max load)}} = \frac{12.7V - 12.6V}{12.6V} * 100 = 0.83\%$$
 (4.13)

Figure 4-6 shows the efficiency of the system ranging from a minimum load current of 0.4A up to full load current of 2A in increments of 0.4A. Table 4-1 shows the power dissipation as well as the efficiency report of the charging flyback at full load. An overall power dissipation table will be used to size the components of the entire bi-directional DC-DC converter. The simulations results for the charging flyback meet the design specifications detailed in Chapter 3.

Table 4-1: Efficiency and Power Dissipation of Components for Charging Flyback at Full Load (2A)

Efficiency: 93.4%			
Input: 27W @ 48V			
Output: 25.2W @ 12.6V			
Ref.	Irms	Ipeak	Dissipation
C1	0mA	0mA	0mW
C2	45mA	1226mA	0mW
C3	2913mA	7360mA	0mW
C4	0mA	0mA	0mW
C5	0mA	7mA	0mW
D1	3535mA	9360mA	864mW
L1	937mA	2374mA	466mW
L2	3535mA	9360mA	29mW
Q1	937mA	2374mA	204mW
R1	0mA	0mA	5μW
R2	0mA	0mA	9mW
R3	0mA	0mA	127µW
R4	0mA	0mA	0μW
R5	0mA	0mA	5mW
R6	0mA	0mA	194µW
R7	933mA	2371mA	29mW
R8	0mA	7mA	0μW
U1	71mA	1273mA	181mW

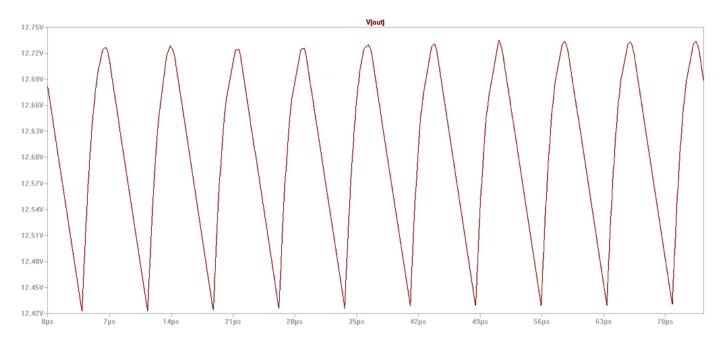


Figure 4-4: Simulated Output Voltage Peak-to-Peak Ripple at Full Load (2A) for Charging Flyback

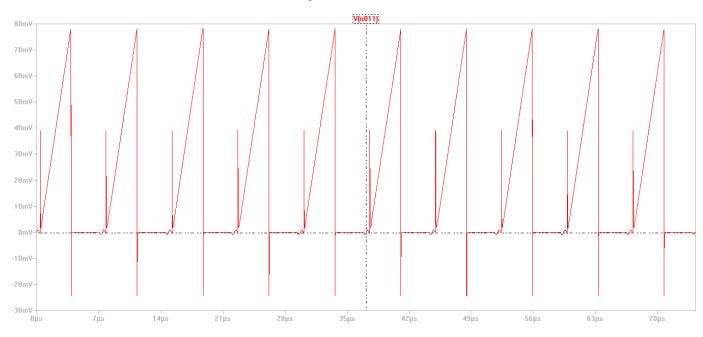


Figure 4-5: Simulated Voltage at Sense Pin at Full Load (2A) for Charging Flyback

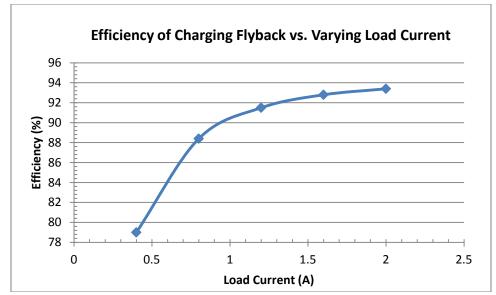


Figure 4-6: Efficiency of the Charging Flyback with Varying Load Current from 0.4A to 2A

4.3. Flyback Design for Discharging Stage

Based upon the design requirements stated in Chapter 3, the discharging stage of the bidirectional DC-DC converter must be able to output a maximum of 60W. Because of the reduced number of components used as well as the lack of feedback or compensation connection on the secondary side of the flyback, the same controller chip (LT3748) used for the charging stage will also be used for the discharging stage. As stated earlier in this chapter, the LT3748 derives the information from the output voltage based upon the primary-side flyback pulse waveform [27]. Similar design equations used for the charging flyback will be used for the discharging flyback for component selection and sizing.

The turns ratio for the transformer was determined to be 4:1 based upon the input voltage and output voltage for the charging flyback. Using the same transformer for the discharging flyback, the turns ratio is determined to be 1:4.

The duty cycle of the flyback can be determined using the following equation given from the LT3748 datasheet [27]:

$$D = \frac{(V_{out} + V_{F(diode)}) * N_{PS}}{V_{in} + (V_{out} + V_{F(diode)}) * N_{PS}}$$
(4.1)

where N_{PS} is the turns ratio N_p/N_s , $V_{F (diode)}$ is the forward voltage drop across the output diode, V_{in} is the input voltage of the flyback, and V_{out} is the output voltage of the flyback. Assuming a forward voltage drop of 1V, input voltage of 12V, a turns ratio of 0.25, and an output voltage of 48V, the nominal duty cycle is approximately 51%.

The LT3748 uses a sense resistor to optimize the current limit of the primary side current. Using the following equation given by the datasheet [27]:

$$R_{sense} = \frac{100 \, mV}{I_{Lmin}} \tag{4.2}$$

$$I_{Lmin} = I_{o(max)} * \frac{2}{N_{PS} * 0.85 * (1-D)}$$
(4.3)

where I_{Lmin} is the minimum peak inductance current on the primary side of the transformer. The minimum peak primary current can be determined using Equation 4.3 from the maximum output current $I_{o(max)}$, the turns ratio N_{PS} , and the duty cycle D. With a maximum output current of 1.2A, a turns ratio of 0.25, and a maximum duty cycle of 0.51, the minimum primary peak inductance current was determined to be 23.5A.

For headroom purposes, the primary inductance peak current used to determine the R_{sense} value is rounded up to 25A. Assuming an I_{Lmin} value of 25A, the R_{sense} value was determined to be 5m Ω . A 100 Ω resistor will be connected in series from the SENSE pin to the sense resistor with a 10000pF capacitor connected in parallel across the sense resistor to provide a cutoff frequency of 160 kHz to reduce noise interference from other components.

The same primary inductance requirements for the LT3748 on the charging flyback must be also be met for the LT3748 on the discharging flyback. As stated earlier for the charging flyback, the LT3748 obtains output voltage information from the external MOSFET drain voltage when the secondary winding conducts current. The sampling circuitry requires a minimum of 300ns to settle and sample the output voltage while the MOSFET switch is off [27]. This required settle and sample time is controlled by external components independent of the minimum off-time of the GATE pin. Therefore, the primary inductance must satisfy the following equation obtained from the datasheet:

$$L_{PRI} \ge \frac{(V_{out} + V_{F(diode)}) * R_{sense} * N * t_{settle(min)}}{V_{sense(min)}}$$
(4.4)

where N is the turns ratio of the transformer, V_{out} is the output voltage, $V_{F(diode)}$ is the forward voltage drop of the output diode, $t_{settle (min)}$ is the settle time for the controller, and $V_{sense (min)}$ is the minimum voltage for the sense pin. Assuming a forward voltage drop of 1V, output voltage of 48V, a turns ratio of 0.25, a sense resistor of 5m Ω , a settle time of 400ns, and a minimum sense voltage of 15mV, the minimum primary inductance must be greater than 1.63 uH.

Besides the primary inductance requirement for minimum settling and sampling time, the LT3748 has internal circuit constraints that prevent it from setting the GATE node high for shorter than approximately 250 ns [27]. The primary inductance must also satisfy the following equation obtained from the datasheet:

$$L_{PRI} \ge \frac{V_{in\,(\text{max})} * R_{sense} * t_{on(\text{min})}}{V_{sense\,(\text{min})}}$$
(4.3)

where $V_{in(max)}$ is the maximum input voltage, R_{sense} is the sense resistor of the SENSE pin, V_{sense} (min) is the minimum sense voltage for the SENSE pin, and $t_{on (min)}$ is the minimum on time of the GATE pin. Assuming a maximum input voltage of 13V, a sense resistor of 5m Ω , a suggested minimum on time of 250ns, and a minimum sense voltage of 15mV, the minimum primary inductance for preventing the setting of the GATE node to be high for shorter than 250ns must be greater than 1.08 uH. The final constraint on the minimum inductance is related to the full-load operating frequency, f_{min} [27]. The final constraint for the primary inductance value must satisfy the following equation obtained from the datasheet:

$$L_{PRI} \le \frac{V_{in\,(\min)} * N_{PS} * (V_{out} + V_{F\,(diode)})}{f_{SW\,(\min)} * I_{Lmin} * (N_{PS} * (V_{out} + V_{F\,(diode)}) + V_{in\,(\min)}}$$
(4.4)

where $V_{in (min}$ is the minimum input voltage, N_{PS} is the turns ratio of the transformer, V_{out} is the output voltage, $V_{F (diode)}$ is the forward voltage drop across the output diode, $f_{SW (min)}$ is the minimum switching frequency for maximum load, and I_{Lmin} is the minimum primary inductance current.

Assuming a minimum input voltage of 12V, a turns ratio of 0.25, an output voltage of 48V, a forward diode voltage drop of 1V, a minimum switching frequency of 42 kHz from the datasheet, and a minimum primary inductance current of 25A, the primary inductance related to full-load operating frequency must not be greater than 11.4 uH. Based upon the secondary inductance value determined from the primary inductance requirements for the charging flyback, the 4.375uH secondary inductance is suitable to be used as the primary inductance of the discharging flyback.

The output diode and MOSFET must be properly sized based upon the following two equations given in the datasheet [27]. The theoretical maximum drain-source voltage is given in Equation 4.6 while the theoretical maximum output diode reverse voltage is given in Equation 4.7:

$$V_{DS(\max)} = V_{in\,(\max)} + V_{out(\max)} * N_{PS}$$
(4.6)

$$V_{RRM} = V_{out(\max)} + \left(\frac{V_{in(\max)}}{N_{PS}}\right)$$
(4.7)

Assuming a nominal input voltage of 12V, a nominal output voltage of 48V, and a turns ratio of 0.25, the theoretical maximum drain-source voltage is 24V and the theoretical maximum output

diode reverse voltage is 96V. In order to maximize the efficiency of the flyback, the MOSFET chosen must be within the rated drain-source voltage but with minimal R_{DS} (on) and the output diode must be within the rated maximum output diode reverse voltage but with a minimal forward diode voltage drop.

Based upon these calculations and the minimum primary inductance current of 25A, the discharging flyback will be implementing an International Rectifier IRFB4127 NMOSFET rated at 200 V_{DS} and a continuous drain current of 76A. The discharging flyback will be implementing a LQA30T300 Schottky output diode rated at 300V. Leakage inductance and voltage spikes were taken into consideration when selecting the output diode and MOSFET switch. For simulation purposes, a MBRB2545CT Schottky diode is used to substitute the LQA30T300 Schottky diode, and a Si4490DY NMOSFET will be used to substitute the IRFB4127 NMOSFET.

Properly sizing the output capacitor is critical to the output voltage peak to peak ripple. Based upon the specifications stated in Chapter 3, the minimum output capacitance value can be calculated based upon the following equation [28]:

$$C_{min} = \frac{D}{R_{min} * f_{min} * \frac{\Delta V}{V_o}}$$
(4.8)

where D is the duty cycle of the flyback, R_{min} is the resistance with full load current, f_{min} is the minimum frequency at worst case scenario, and $\Delta V/V_o$ is the peak to peak ripple. Using a duty cycle of 51%, an R_{min} of 40 Ω , a worst case switching frequency of 42 kHz [27], and a peak to peak ripple of 5%, the minimum capacitance required is calculated to be 6.07 uF. For the discharging flyback, three 10uF X7R capacitors will be connected in parallel with a rated voltage of 50V, creating an overall output capacitance of 30uF. Connecting the capacitors in parallel will reduce the ESR of the output capacitance which helps the overall efficiency of the discharging flyback.

The LT3748 derives the output voltage by a resistor ratio between the feedback resistor on the primary side of the transformer and a reference resistor [27]. The reference resistor, ranging from 5.76k Ω to 6.34k Ω , is suggested to be nominally set at 6.04k Ω . Using the following equation obtained from the datasheet, the feedback resistor (R_{FB}) is determined to be [27]:

$$R_{FB} = \frac{V_{out}}{V_{BG}} * N_{PS} * R_{REF}$$
(4.9)

where V_{out} is the output voltage, N_{PS} is the turns ratio, R_{REF} is the reference resistor, and V_{BG} is the bandgap voltage of 1.223V that is the reference voltage of the error amplifier within the controller. With an output voltage of 48V, a reference resistor of 6.04k Ω , and a turns ratio of 0.25, the feedback resistor is calculated to be 59k Ω .

The LT3748 allows an enable/undervoltage lockout feature to protect the circuit if the input voltage is under the minimum input voltage of the controller. A resistive divider is formed from the input voltage line to the EN/UVLO pin to create a reference voltage that is compared to the pin threshold voltage of 1.223V [27]. If the reference voltage from the resistive divider is greater than or equal to the threshold voltage, the EN/UVLO will allow the controller chip to operate. Using the following equations obtained from the datasheet, the resistive divider is determined to be:

$$1.223V = 10.5V * \left(\frac{R_2}{R_1 + R_2}\right) \tag{4.11}$$

10.5V is chosen as the minimum voltage possible for the input of the discharging flyback based upon the minimum voltage of the lead-acid battery when the cells are completely depleted. The resistive value for R_1 was determined to be $1.4k\Omega$ and the resistive value for R_2 was determined to be $10k\Omega$. This ENABLE/UVLO pin will be used later on to control both the charging and discharging flyback. The LT3748 uses an external resistor-capacitor network to compensate for the loop gain [27]. Typical values suggested by the datasheet are in the range of $R_C = 50k\Omega$ and $C_C = 1nF$. If the resistor value for R_C is too large, the transient performance is most susceptible to high frequency noise and jitter. If too small, the transient performance will suffer as well. The value choice for C_C is the inverse of the value choice for R_C : if too small of a value, the loop may be unstable and if too large of a value, the transient performance will suffer. Based upon these guidelines, a suitable 10k Ω resistor and 4.7 nF capacitor was chosen for loop compensation.

The INTV_{cc} pin is the input voltage pin that powers the internal circuitry of the LT3748. Based upon the suggested configurations given in the LT3748 datasheet, a capacitor will be connected in series to ground because an external power supply will be used to provide power to the entire circuit. Connected a capacitor in series with the INTV_{cc} pin will provide a more efficient source of power for internal circuitry and reduce power dissipation in the LT3748 chip [27].

Figure 4-7 shows the complete 12V to 48V discharging flyback with calculated resistors and capacitors for each pin of the controller chip. It is important to note that the soft-start pin and output voltage temperature compensation pins are used in this configuration in order to optimize the performance of the charging flyback. Because the soft-start and output voltage temperature compensation are extra features of the controller that are not necessary for charging, calculations and design options were not detailed in this chapter.

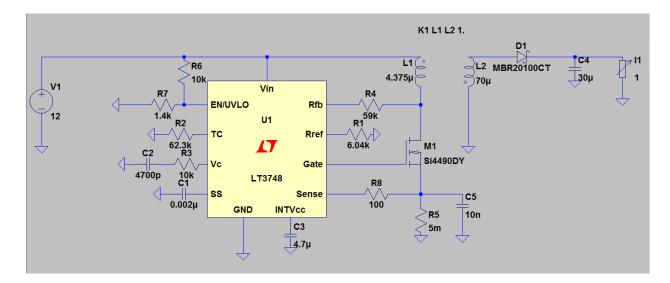


Figure 4-7: 12V to 48V Discharging Flyback with LT3748 Controller Chip

4.4. Flyback Design Simulation Results for Discharging Stage

Figure 4-8 shows the output voltage ripple for the discharging flyback with a full load of 1A. The average voltage is observed to be 48.3V, with a peak to peak ripple voltage of 0.4V or 0.83% of the output voltage. Figure 4-9 shows the voltage of the current sense pin of the LT3748 controller when the discharging flyback is supplying power for full load. Boundary conduction mode can be seen as the voltage of the current sense pin drops to zero. Table 4-2 shows the power dissipation and efficiency of the discharging flyback at full load. Figure 4-10 shows the efficiency of the discharging flyback from 0.2A to 1A load current in increments of 0.2A. The simulations results for the charging flyback meet the design specifications detailed in Chapter 3.

The line regulation of the charging flyback is determined using Equation 4.14:

$$Line Regulation = \frac{V_{o(high-input)} - V_{o(low-input)}}{V_{o(nom input)}} = \frac{48.4V - 48.4V}{48.4V} * 100 = 0\%$$
(4.14)

The load regulation of the charging flyback is determined using Equation 4.15:

Load Regulation =
$$\frac{V_{o(\min load)} - V_{o(\max load)}}{V_{o(\max load)}} = \frac{48.4V - 48.3V}{48.4V} * 100 = 0.83\%$$
 (4.15)

	Full Load (1	lA)	
Efficiency: 91.9%			
Input: 52.6W @ 12V			
Output: 48.4W @ 48.4V			
Ref.	Irms	Ipeak	Dissipation
C1	0mA	0mA	0mW
C2	0mA	0mA	0mW
C3	24mA	1263mA	0mW
C4	1342mA	3245mA	0mW
C5	5mA	1431mA	0mW
D1	1667mA	4245mA	579mW
L1	6996mA	17009mA	0mW
L2	1667mA	4245mA	0mW
M1	6996mA	17009mA	3429mW
R1	0mA	0mA	131µW
R2	0mA	0mA	5µW
R3	0mA	0mA	0µW
R4	0mA	0mA	2mW
R5	6995mA	17004mA	245mW
R6	1mA	1mA	11mW
R7	1mA	1mA	2mW

 Table 4-2: Efficiency and Power Dissipation of Components for Discharging Flyback at Full Load (1A)

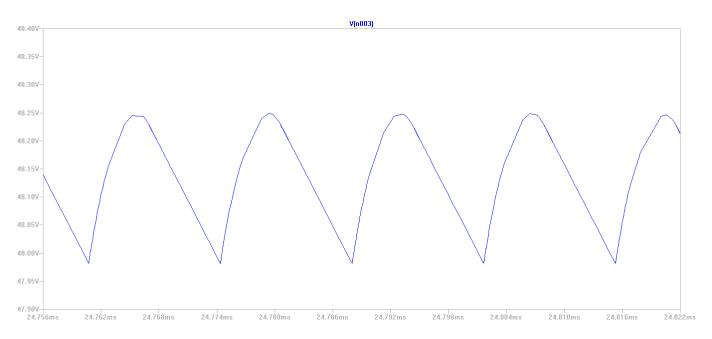


Figure 4-8: Simulated Output Voltage Peak-to-Peak Ripple for 1A Load for Discharging Flyback

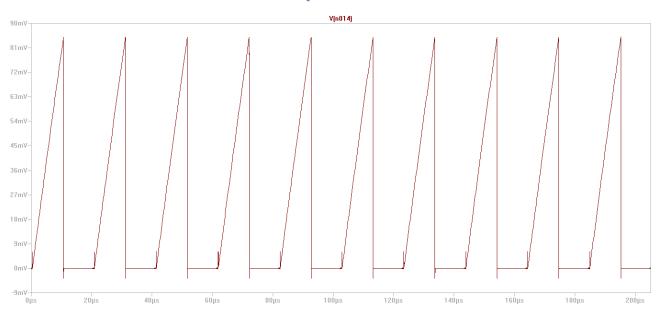


Figure 4-9: Simulated Voltage at Sense Pin at Full Load (1A) for Discharging Flyback

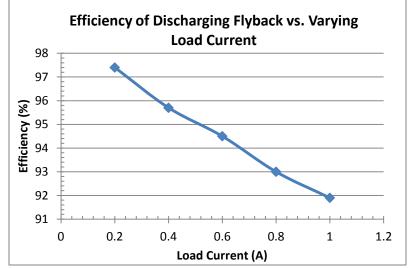


Figure 4-10: Efficiency of Discharging Flyback vs. Varying Load Current

4.5. Bi-directional Flyback Control Scheme Design

As stated earlier in the design of the charging flyback and discharging flyback, a proper control scheme will be used to utilize the ENABLE/UVLO pins of both LT3748 controller chips. Figure 4-11 shows that connecting a MOSFET in parallel with the second resistor in the resistor network connected at the ENABLE/UVLO pin of the LT3748 provides a shutdown option that turns off the controller chip.

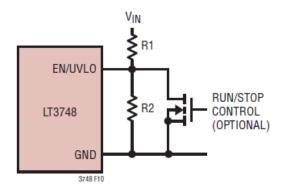


Figure 4-11: Shutdown Option at EN/UVLO pin of LT3748 [27]

Based upon the voltage level of the lead-acid battery, the control scheme will be able to tell which controller chip to operate based upon the battery's need to charge or ability to discharge. A voltage will be used to bias the MOSFET switch to turn off one controller chip, while the other controller chip takes the same voltage to provide the necessary 1.223V to enable the gate voltage pin to pulsate.

Based upon these requirements, the LT1716 is chosen as the comparator chip because of its large input voltage range (2.7V to 44V), its low profile packaging, as well as its small current draw resulting in micropower usage [29]. In order to properly design the control scheme using the LT1716, bias and input voltages must be determined in order to properly turn either the discharging or charging flyback properly.

Because the lead acid battery should not be completely depleted, a set voltage will be used as a reference voltage within a comparator to compare the lead acid battery voltage with. A depleted lead-acid battery will typically output 10V, thus the set voltage of 11V will be used to compare with the lead-acid battery voltage. When the lead-acid battery voltage level is above 11V, the LT1716 will send the bias voltage as an output to shut down the discharging LT3748 controller to allow the charging LT3748 controller to turn on. When the lead-acid battery voltage level falls below 11V, the LT1716 does not send any output voltage, disabling the discharging LT3748 controller and does not provide a bias voltage for the MOSFET on the resistive network of the charging LT3748 EN/UVLO pin. This allows the charging LT3748 controller chip to turn on. The bias voltage and set voltage will be provided by power supplies to simulate the 48V DC bus line providing the voltages to the LT1716. Figure 4-12 shows the LT1716 with the biasing voltage, set voltage, and voltage source imitating the lead-acid battery.

An IRFH6200 NMOSFET is chosen to be placed in parallel with the second resistor in the resistive divider on the EN/UVLO pin. The IRFH6200 offers a lower $R_{DS(on)}$ resistance as well as a low 3V gate-source biasing voltage needed to turn on the NMOSFET. Because the

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LT1716 is providing a small amount of current at the output, the IRFH6200 will not be affecting the efficiency of bi-directional DC-DC converter.

Figures 4-13 shows output voltage of the LT1716 when the battery level is above the 11V threshold and ready to discharge power. The output voltage of 16V will bias the shutdown MOSFET, turning off the charging flyback. Figure 4-14 shows the output voltage of the LT1716 when the battery level is below 11V and requires charging. An output voltage of 0V does not provide the proper voltage for the ENABLE/UVLO resistive divider which shuts down the discharging flyback.

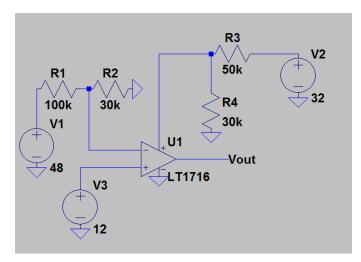
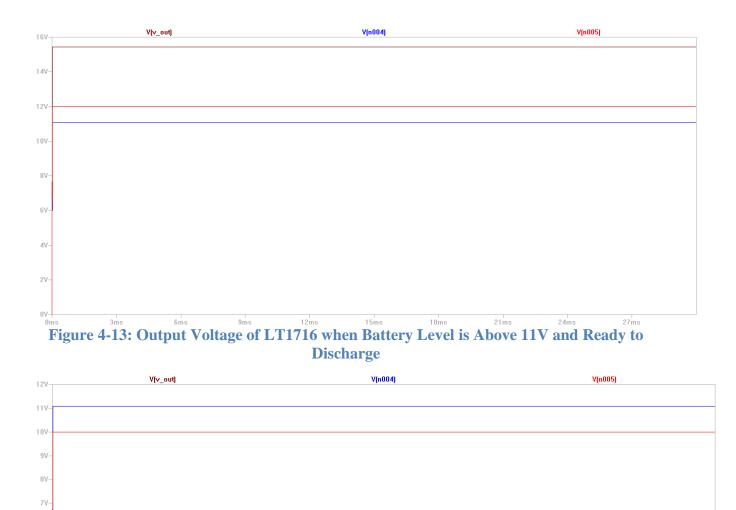


Figure 4-12: LT1716 Schematic for Bi-Directional Control Scheme





4.6. Full Bi-directional DC-DC Converter Design and Simulation Results

6V-5V-4V-3V-2V-1V-0V-

Figure 4-15 shows the entire bi-directional DC-DC converter design with the complete

LT1716 control scheme. In order to simulate each flyback separately, the load and main input

voltage source is alternated between the inputs of each controller chip. A separate voltage source

is used for one of the inputs of the LT1716 to emulate the voltage level of the battery. The placement of the output diodes are placed across the MOSFET switches of each flyback to fulfill the bi-directional format.

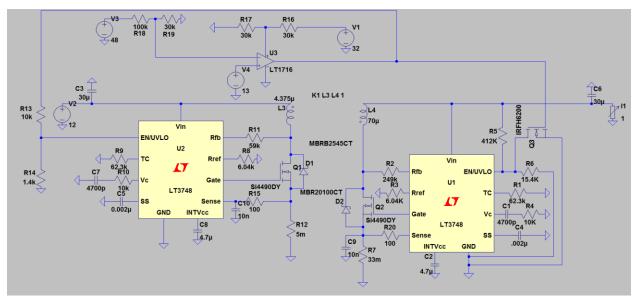


Figure 4-15: Full Bi-directional DC-DC Converter LT Spice Design

Figure 4-16 shows the output voltage peak-to-peak ripple for the discharging flyback for a full load of 1A. The average output voltage of the discharging flyback is 48.3V, with a peak-topeak voltage ripple of 0.3V or 0.61% of the output voltage. Figure 4-17 shows the gate pin voltages of both controllers, showing that since the EN/UVLO pin of the charging LT3748 controller chip is below 1.223V, the gate voltage pin of the charging flyback is off.

Table 4-3 shows the power dissipation of all components during the operation of the discharging flyback, as well as the input power, output power, output voltage, and overall efficiency of the bi-directional converter when the discharging flyback is supplying power for full load. The largest power dissipation value from either the operation of the charging flyback or discharging flyback will be used to size the components.

The load regulation for the discharging flyback is determined based upon the difference between the output voltage seen at full load (1A) and the output voltage seen at minimum load (0.2A) divided by the nominal output voltage of the flyback. The output voltage at maximum load and minimum load are 48.3V and 48.3V respectively. Equation 4.16 shows the load regulation of the discharging flyback:

Load Regulation =
$$\frac{(V_{o(\min load)} - V_{o(\max load)})}{V_{o(\max load)}} * 100 = \frac{48.3V - 48.3V}{48.3V} * 100 = 0\%$$
 (4.16)

Line regulation for the discharging flyback is determined to be the output voltage at high input voltage of 13V minus the output voltage at low input voltage of 10.5V divided by the nominal output voltage. Line regulation is calculated during full load operation. The output voltage at high input voltage and output voltage at low input voltage are 48.3V and 48.2 V respectively. Equation 4.17 shows the line regulation of the discharging flyback:

$$Line \ Regulation = \frac{(V_{o(high-input)} - V_{o(low-input)})}{V_{o(nom \ input)}} * 100 = \frac{48.3V - 48.2V}{48.3V} * 100 = 0.2\%$$
(4.17)

Figure 4-18 shows the efficiency of the discharging flyback of the bi-directional converter starting from 0.2A load current to 1A full load in increments of 0.2A. The simulation results of the discharging flyback matches the design specifications stated in Chapter 3.

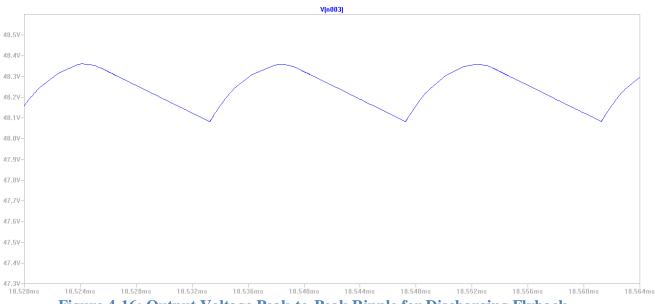


Figure 4-16: Output Voltage Peak-to-Peak Ripple for Discharging Flyback

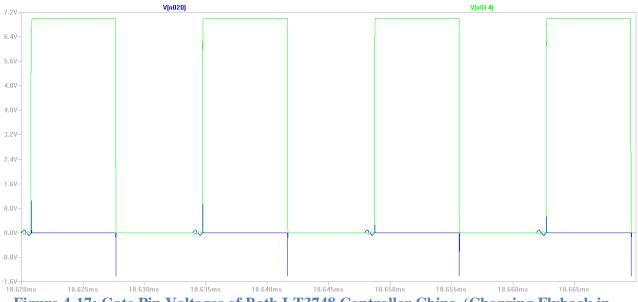


Figure 4-17: Gate Pin Voltages of Both LT3748 Controller Chips, (Charging Flyback in Blue, Discharging Flyback in Green)

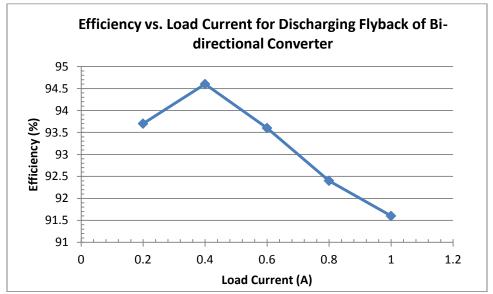


Figure 4-18: Efficiency vs. Load Current of Discharging Flyback for Bi-Directional Converter

Efficiency: 91.6%			
Input: 52.7W @ 12V			
Output: 48.3W @ 48.3V			
Ref.	Irms	Ipeak	Dissipation
C1	0mA	0mA	0mW
C2	0mA	1mA	0mW
C3	0mA	0mA	0mW
C4	0mA	0mA	0mW
C5	0mA	0mA	0mW
C6	1303mA	3454mA	0mW
C7	0mA	0mA	0mW
C8	35mA	1233mA	0mW
С9	5mA	265mA	0mW
C10	4mA	351mA	0mW
D1	52mA	2160mA	0mW
D2	1309mA	3824mA	385mW
L3	7349mA	17873mA	0mW
L4	1464mA	4455mA	0mW
Q1	7349mA	17883mA	3860mW
Q2	173mA	4124mA	38mW
Q3	0mA	0mA	0mW
R1	0mA	0mA	0µW
R2	0mA	0mA	8mW
R3	0mA	0mA	0µW

Table 4-3: Efficiency and Power Dissipation of Components of Bi-Directional Converterduring Operation of Discharging Flyback at Full Load (1A)

0mA	0mA	0µW
0mA	0mA	6mW
0mA	0mA	0µW
1462mA	4418mA	71mW
0mA	0mA	98µW
0mA	0mA	5μW
0mA	0mA	0µW
0mA	0mA	2mW
7348mA	17839mA	270mW
1mA	1mA	11mW
1mA	1mA	2mW
0mA	0mA	0µW
0mA	0mA	0µW
23mA	713mA	2mW
46mA	1290mA	17mW
0mA	0mA	0mW
0mA	1mA	0mW
		0mW
0mA	0mA	0mW
0mA	0mA	0mW
	0mA 0mA 1462mA 0mA 0mA 0mA 0mA 7348mA 1mA 1mA 1mA 0mA 0mA 23mA 46mA 0mA 0mA 0mA 0mA	0mA 0mA 0mA 0mA 1462mA 4418mA 0mA 0mA 1mA 1mA 1mA 1mA 0mA 0mA 0mA 0mA

Figure 4-19 shows the output voltage peak-to-peak ripple for the charging flyback for a full load of 2A. The average output voltage of the charging flyback is 12.6V, with a peak-to-peak voltage ripple of 0.3V or 2.4% of the output voltage. Figure 4-20 shows the gate pin voltages of both controllers, showing that since the EN/UVLO pin of the discharging LT3748 controller chip is below 1.223V, the gate voltage pin of the discharging flyback is off.

Table 4-4 shows the power dissipation of all components during the operation of the charging flyback, as well as the input power, output power, output voltage, and overall efficiency of the bi-directional converter when the charging flyback is supplying power for full load.

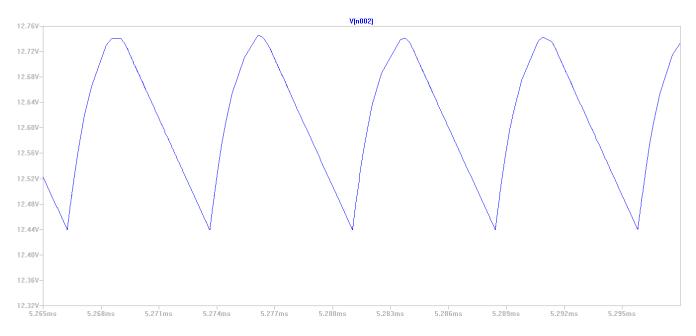
The load regulation for the charging flyback is determined based upon the difference between the output voltage seen at full load (2A) and the output voltage seen at minimum load (0.1A) divided by the nominal output voltage of the flyback. The output voltage at maximum load and minimum load are 12.6V and 12.7V respectively. Equation 4.18 shows the load regulation of the charging flyback:

Load Regulation =
$$\frac{(V_{o(\min load)} - V_{o(\max load)})}{V_{o(\max load)}} * 100 = \frac{12.7V - 12.6V}{12.6V} * 100 = 0.7\%$$
 (4.18)

Line regulation for the charging flyback is determined to be the output voltage at high input voltage of 50V minus the output voltage at low input voltage of 46V divided by the nominal output voltage. Line regulation is calculated during full load operation. The output voltage at high input voltage and output voltage at low input voltage are 12.6V and 12.6V respectively. Equation 4.19 shows the line regulation of the charging flyback:

$$Line \ Regulation = \frac{(V_{o(high-input)} - V_{o(low-input)})}{V_{o(nom \ input)}} * 100 = \frac{12.6V - 12.6V}{12.6V} * 100 = 0\%$$
(4.19)

Figure 4-21 shows the efficiency of the charging flyback of the bi-directional converter starting from 0.4A load current to 2A full load in increments of 0.4A. The simulation results of the charging flyback matches the design specifications stated in Chapter 3.





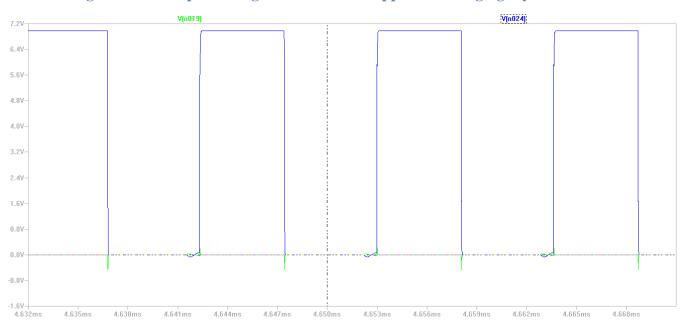


Figure 4-20: Gate Pin Voltages of Both LT3748 Controller Chips, (Charging Flyback in Blue, Discharging Flyback in Green)

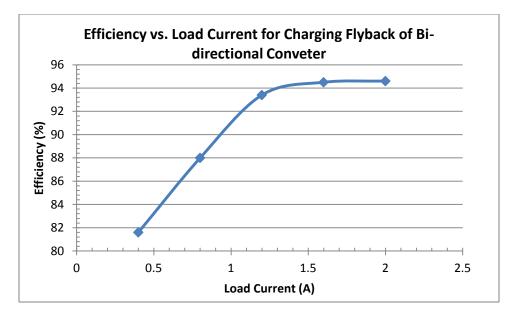


Figure 4-21: Efficiency vs. Load Current for Charging Flyback of Bi-Directional Converter

Table 4-4: Efficiency and Power Dissipation of Components of Bi-Directional Converter
during Operation of Charging Flyback at Full Load (2A)

Efficiency: 94.6%			
Input: 26.6W @ 48V			
Output: 25.2W @ 12.6V			
Ref.	Irms	Ipeak	Dissipation
C1	0mA	0mA	0mW
C2	38mA	1186mA	0mW
C3	2785mA	6935mA	0mW
C4	0mA	0mA	0mW
C5	0mA	0mA	0mW
C6	0mA	0mA	0mW
C7	0mA	0mA	0mW
C8	0mA	0mA	0mW
С9	0mA	4mA	0mW

C10	0mA	3mA	0mW
D1	3400mA	8919mA	834mW
D2	1mA	15mA	6mW
L3	3401mA	8935mA	0mW
L4	907mA	2265mA	0mW
Q1	25mA	1342mA	0mW
Q2	907mA	2265mA	152mW
Q3	0mA	0mA	0mW
R1	0mA	0mA	5µW
R2	0mA	0mA	9mW
R3	0mA	0mA	130µW
R4	0mA	0mA	0µW
R5	0mA	0mA	5mW
R6	0mA	0mA	194µW
R7	905mA	2262mA	16mW
R8	0mA	0mA	0µW
R9	0mA	0mA	0µW
R10	0mA	0mA	0µW
R11	0mA	0mA	2mW
R12	3400mA	8908mA	58mW
R13	0mA	0mA	0µW
R14	0mA	0mA	0µW
R15	0mA	3mA	0µW
R16	0mA	0mA	9mW
R17	0mA	0mA	4mW

R18	0mA	0mA	14mW
R19	0mA	0mA	4mW
R20	0mA	4mA	0μW
U1	0mA	0mA	129mW
U2	0mA	0mA	1mW
U3	0mA	0mA	2mW

Table 4-5 shows a summary of the simulation results of both charging and discharging stages of the bi-directional DC-DC converter at full load conditions compared to the design requirements stated in Chapter 3. As seen in Table 4-5, all simulation results for both charging and discharging flybacks of the bi-directional converter meet the specifications stated in Chapter 3.

	Charging Stage		Discharging Stage	
	Design	Simulation	Design	Simulation
	Requirement	Results	Requirement	Results
Input Voltage	48V	48V	12V	12V
Output Voltage	12.5V	12.6V	48V	48.3V
Full Load Current	2A	2A	1A	1A
Full Load Output				
Wattage	25W	27W	48W	53W
Line Regulation	5%	0%	5%	0%
Load Regulation	5%	0.7%	5%	0.2%
Output Voltage				
Ripple	5%	2.4%	5%	0.3%
Efficiency at Full				
Load	$\geq 80\%$	95%	$\geq 80\%$	92%

Table 4-5: Simulation Results and Design Requirements Summary

4.7. Bi-directional Flyback Transformer Design

The LT3748 uses boundary conduction mode to provide current mode switching for the isolated flyback. However, designing the flyback transformer in continuous conduction mode covers boundary conduction operation and allows increased power capability for the bidirectional converter. Therefore, for the design of the transformer, continuous conduction mode considerations will be used. A starting point for primary and secondary inductance values was discussed earlier in this chapter based upon the primary inductance requirements of both the discharging and charging flyback. However, since the power ratings for the discharging flyback is higher than the power ratings of the charging flyback, the flyback transformer will be designed using the 4.375uH as the primary inductance value of the flyback transformer and 70uH as the secondary inductance value of the flyback transformer.

Table 4-6 shows electrical parameters used to determine the proper core selection for the flyback transformer [30 - 32]. These electrical parameters are based upon the discharging flyback of the bi-directional converter. The switching frequency selected is based upon the optimized switching frequency given in the LT3748 datasheet under design suggestions [27].

Minimum Input Voltage	10.5V
Maximum Input Voltage	13V
Switching Frequency	100 kHz
Output Voltage	48V
Output Power	60W
Primary Inductance	4.375uH
Turns Ratio (N _P /N _S)	1:4

Table 4-6: Initial Elect	rical Parameters for	r Flyback	Transformer Design

There are several different types of cores that can be used for a transformer. Ferrite cores offer the benefits of low losses, low cost, and a wide variety of available shapes and sizes [35]. Pot cores offer the advantage of protective shielding which can be important in EMI/RF sensitive designs [35]. Planar E cores offer ease of assembly, consistent electrical results, and a low profile [35]. Tape wound cores have a higher flux density and higher saturation flux density than most cores while providing a smaller overall design [35]. Because efficiency and low costs are two advantages that are beneficial for the bi-directional DC-DC converter, ferrite cores are chosen for as the core selection for the bi-directional DC-DC converter flyback transformer.

In order to determine the proper core for the transformer, the minimum core size and the material of the core must be determined. Figure 4-22 shows a graph showing core losses based upon temperature for different materials of ferrite cores [34]. From the figure, R material provides the lowest core losses for the same temperature range compared to other ferrite material cores. For the bi-directional DC-DC converter transformer design, R material ferrite cores will be considered.

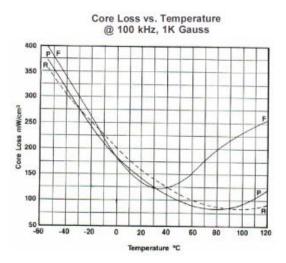


Figure 4-22: Core Losses versus Temperature for Different Material Ferrite Cores [34]

The minimum core size will be determined using the area product method [30]. Equation 4.13 details the area product equation, which requires the primary peak current $I_{p(peak)}$, the primary RMS current $I_{p(rms)}$, the winding factor k, and the maximum flux density of the R material of the ferrite core B_{max} :

$$A_p = \left(\frac{L_p * I_{p(peak)} * I_{p(rms)} * 10^4}{420 * k * B_{max}}\right)$$
(4.13)

The peak-to-peak current seen by the primary inductance can be determined using Euation 4.14 [30]:

$$\Delta I_{Lp} = \frac{\Delta t * (V_{in(min)} - V_{sw(on)})}{L_p} \tag{4.14}$$

where Δt is the change in time during the change of current across the primary inductance, $V_{in(min)}$ is the minimum input voltage of the primary side of the transformer, $V_{SW(on)}$ is the voltage drop across the switch when the switch is on, and L_P is the primary inductance value. Assuming a switch voltage drop of 1V, a minimum input voltage of 10.5V, a primary inductance value of 4.375uH, and a change in time of $1*10^{-5}$ s, the peak-to-peak current is determined to be 25.7A.

The primary peak current $I_{p(peak)}$ can be determined using Equation 4.15 [30]:

$$I_{p(peak)} = \left(\frac{N_s}{N_p} * I_{o(\max)}\right) * \left(\frac{1}{1 - D_{\max}}\right) + \left(\frac{\Delta I_{Lp}}{2}\right)$$
(4.15)

where N_s/N_p is the secondary to primary turns ratio, $I_{o(max)}$ is the maximum output current, D_{max} is the maximum duty cycle of the converter, and ΔI_{Lp} is the peak-to-peak current of the primary current. Assuming a maximum output current of 1.2A, a maximum duty cycle for the discharging flyback of 0.51, a secondary to primary turns ratio of 4, and a peak-to-peak current ripple of 25.7A, the primary peak current is determined to be 29.4A.

The primary RMS current $I_{p(RMS)}$ can be determined using Equation 4.16 [30]:

$$I_{p(RMS)} = \sqrt{\left(\frac{t_{on(max)}}{T}\right) * \left(I_{p(peak)}^2 - \Delta I_{Lp} * I_{p(peak)} + \frac{\Delta I_{Lp}^2}{3}\right)}$$
(4.16)

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where $t_{on (max)}$ is the maximum time the switch is on, T is the switching time period of the converter, $I_{p(peak)}$ is the peak primary current, and ΔI_{Lp} is the peak-to-peak current ripple of the primary inductor. Assuming a primary peak current of 29.4A, a peak-to-peak current ripple of 25.7A, a switching time period of $1*10^{-5}$ s, and a maximum on time of $5.25*10^{-6}$, the primary RMS current is determined to be 13.3A.

With the primary peak current and primary RMS current calculated, the estimated area product of the transformer can be calculated using Equation 4.17:

$$A_p = \left(\frac{4.375\mu H * 29.4A * 13.3A * 10^4}{420 * 0.2 * 0.3T}\right) = 0.678 \ cm^4 \tag{4.17}$$

The maximum flux density of an R material ferrite core is determined to be 0.3 mT [33]. For a continuous flyback, the winding factor k is equal to 0.2 [30]. With a primary peak current of 29.4A, a primary RMS current of 13.3A, and a primary inductance of 4.375uH, the estimated area product is determined to be 0.678 cm⁴.

With the estimated area product determined, a table of R material ferrite cores and their corresponding area product values is used to determine the proper ferrite core for the bidirectional converter [36]. Based upon the table, the PQ3535 core is selected because its larger area product value (2.00 cm^4) compared to the calculated area product value (0.678 cm^4) .

With the core selected, the minimum number of turns for the primary and secondary of the transformer must be determined based upon the B_{max} and the effective core area of the PQ3535. Based upon the PQ3535 datasheet shown in Appendix A, the maximum flux density is determined to be 0.3 mT and the effective core area was determined to be 1.90 cm². Using Equation 4.18, the minimum number of primary turns can be determined [30]:

$$N_p = \frac{L_p * (I_{p(peak)} * 10^4)}{B_{max} * A_e}$$
(4.18)

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where L_p is the primary inductance, $I_{p (peak)}$ is the primary peak current, B_{max} is the maximum flux density of the PQ3535 core and A_e is the effective core area. With a primary inductance of 4.375uH, a primary peak current of 29.4 A, a B_{max} of 0.3T, and an effective core area of 1.9 cm², the minimum number of primary turns was determined to be 2.257 turns. The minimum number of primary turns is rounded to the nearest integer, making it turns to be close to 3 turns.

The secondary turns ratio can be determined by multiplying the minimum primary turns by the desired turns ratio. With a turns ratio of 1 primary turn to 4 secondary turns, the minimum secondary turns is determined to be 12 turns.

Air-gaps are essential in a flyback transformer because energy is stored in the air-gaps due to the high permeability of the ferrite material causing the material to not store much energy without saturating first [30]. The size of the air-gap in centimeters can be determined using Equation 4.19 [30]:

$$l_g = \frac{\mu_r * \mu_o * N_p^2 * A_e * 10^{-2}}{L_p} \tag{4.19}$$

where μ_r is the relative permeability of the R material, μ_o is a constant for free space $(4\pi^*10^{-7} \text{ H/m})$, A_e is the effective core area, N_p is the minimum primary turns, and L_P is the primary inductance. From the R material datasheet, the relative permeability is determined to be 2300 [33]. With a relative permeability of 2300, an effective core area of 1.9 cm², a primary inductance of 4.375uH, and a primary turns of 3, the air gap was determined to be 6.9*10⁻³ cm. The air-gap will be created using Kapton tape, which is 2mil in length. Using a conversion of 1 mil to 0.00254 centimeters, 4 layers of Kapton tape will be used to create the air-gap for the transformer.

A proper gauge wire must be selected for both the primary and secondary windings of the flyback transformer based upon the current density and area product equation. Equation 4.20

shows that current density can be determined based upon a constant for temperature increase of the core and the area product of the core:

$$J = K_i * A_p^{-0.125} \tag{4.20}$$

The constant K_J can be selected based upon the kind of core and expected temperature increase of the transformer. For this flyback transformer, the temperature increase is chosen to be a change of 50°C for the pot core PQ3535. From the table of K_J constants [30], the constant is determined to be 632. Using the area product value calculated earlier in this section, the current density is determined to be 663.4 A/cm².

The bare wire sizings of the primary and secondary windings can be determined using Equations 4.21 and 4.22:

$$AWB_P = \frac{I_P}{J} \tag{4.21}$$

$$AWB_S = \frac{I_o}{J} \tag{4.22}$$

where I_p is the average input current, I_o is the average output current and J is the current density. The average output current is the maximum full load of the discharging flyback which is 2A. The average input current is the average voltage (12V) divided by the output power times the expected efficiency of the flyback. With an expected efficiency of 80% and an output power of 60W, the average input current is determined to be 6.25A. With the average input current, average output current and current density defined the bare wire size for the primary and secondary windings are determined to be 9.4*10⁻³ cm² and 3.0*10⁻³ cm² respectively.

Using the American Wire Gauge table, the gauge wire is selected based upon the bare wire size compared to the conductor diameter. With a bare wire size of $9.4*10^{-3}$ cm², the gauge wire for the primary winding is selected to be 18AWG because of a higher diameter of $1.02*10^{-3}$ cm². With a bare wire size of $3.0*10^{-3}$ cm², the gauge wire for the primary winding is selected to

be 24AWG because of a higher diameter of $5.1*10^{-3}$ cm². Table 4-7 shows a summary of the gauge wire for each winding as well as the number of expected turns for each winding of the flyback transformer.

Table 4-7: Gauge Wire Used and Minimum Turns for Primary and Secondary Windings of
Transformer

	Primary Winding	Secondary Winding
	(4.375uH)	(70uH)
Minimum Turns	3	12
Gauge Wire Used	18AWG	24AWG

Chapter 5 - Hardware Results

The physical implementation of the bi-directional DC-DC converter will be discussed in reference to the design requirements discussed in Chapter 3 and the design results in Chapter 4. Hardware results for the discharging and charging flyback will be shown in this chapter, as well as the PCB Layout and test set-up for the converter. Procedures and data will also be presented for the custom flyback transformer created for the bi-directional DC-DC converter.

5.1. Flyback Transformer

The secondary windings will be the first layer wounded around the bobbin of the PQ3535 core, followed by a layer of the primary windings. Each winding will be wrapped with Kapton tape to create isolation from each winding as well as securing the winding as tight as possible against the bobbin. The primary windings will be using two 18 AWG wires in parallel to help split the current flow in order achieve higher efficiency and lower leakage inductance.



Figure 5-1: Completed Flyback Transformer for Bi-directional Converter

Figure 5-1 shows the completed flyback transformer. Dot orientation was verified by sending a sine wave signal from the function generator on the primary side of the transformer and monitoring the output waveform on the secondary side of the waveform. Since the dot polarity must be reversed for a flyback transformer, the output waveform on the secondary winding will be inverted compared to the input sine waveform on the primary winding. Figures

5-2 and 5-3 showing the primary and secondary inductance values measured at 100 kHz. Although the values measured are larger than the calculated values suggested in previous chapters, the primary and secondary inductance of the transformer still satisfy the primary inductance requirements for both LT3748 controller chips. The inductance ratio of primary to secondary winding is close to 1:16, making the turns ratio be exactly 1:4 primary to secondary.



Figure 5-2: Primary Inductance Value of Flyback Transformer at 100 kHz



Figure 5-3: Secondary Inductance Value of Flyback Transformer at 100 kHz

5.2. Bi-directional DC-DC Converter Layout

The bi-directional DC-DC converter was designed using a PCB layout program provided by ExpressPCB. Common-practice rules for design were followed, including minimum trace spacing and proper trace width dependent upon average current seen by each trace. The PCB layout was designed using 4 layers: top copper layer, power layer, ground layer, and bottom copper layer. Figure 5-4 shows the entire PCB design with the top layer traces and bottom layer traces.

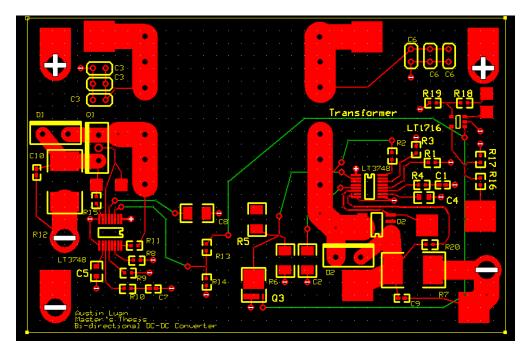


Figure 5-4: Top Layer with Silkscreen and Bottom Layer of PCB

As shown in Figure 5-4, the board is evenly spaced with the location of the two different flyback controllers in the bottom right and bottom left corner of the board, followed by the LT1716 control chip and its resistive networks in the upper right corner of the board, and finally the placement of the transformer in the middle of the board. For each of the controller chips, the input voltage pins to the controller chip are tied to the power plane using vias. All ground connections throughout the board also use vias. The MOSFET and sense resistor of each flyback are placed as close to the controller chip as possible in order to reduce additional noise or interference to the voltage signals. A gate pad of the switching MOSFET and a sense pad at the beginning of the sense resistor are placed for both flybacks in order to easily monitor signals when using an oscilloscope. Pads are also placed with posts to provide inputs for the input of the transformer, the power plane, and the ground plane.

Because some of the traces from the LT1716 will overlap on the top layer, bottom layer traces are used to send the signal of the LT1716 to operate the shutdown MOSFET of the charging flyback and the ENABLE/UVLO pin of the discharging flyback. The feedback resistor's trace for the discharging controller on the left side of the board will also overlap the EN/UVLO and INTV_{CC} traces, making the use of bottom layer traces to connect the controller chip to its corresponding EN/UVLO resistive network and INTV_{CC} capacitor. Figure 5-5 shows the bottom layer with the silkscreen prints to show the location of the LT1716 and the traces to the shutdown MOSFET and EN/UVLO resistive network of the discharging LT3748.

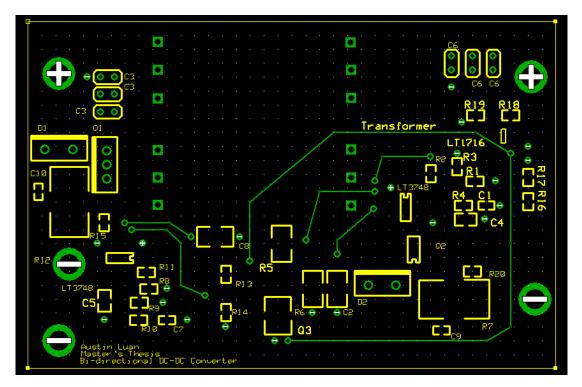


Figure 5-5: Bottom Layer with Layer Traces

5.3. Bi-directional DC-DC Converter Test Set-Up

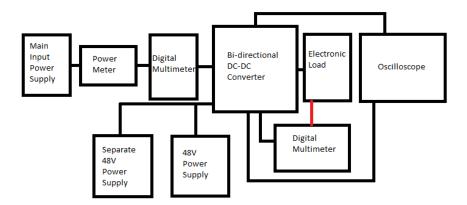


Figure 5-6: Bi-directional DC-DC Converter Test Set-up

Figure 5-6 shows the testing set-up for the bi-directional DC-DC converter. The main input power supply is connected directly to the power meter to monitor the input power, input voltage, and input current being drawn by the converter. However, due to the length of the wires coming out of the main input power supply, a separate digital multimeter will be used to strictly monitor the input current. Two separate power supplies are used to mimic the 48V DC bus line instead of using the same input power supply. An electronic load is connected at the output of the converter which controls the output current sourced by the converter while accurately reading the output power. Because the wires used to connect the load to the output of the converter is lengthy, a separate digital multimeter will be used to accurately monitor the output voltage of the converter. At the end of the test set-up, an oscilloscope or isolated oscilloscope will be used to monitor any voltage waveforms of the converter. Figure 5-8 shows the entire set-up and equipment used for testing the DC-DC converter.

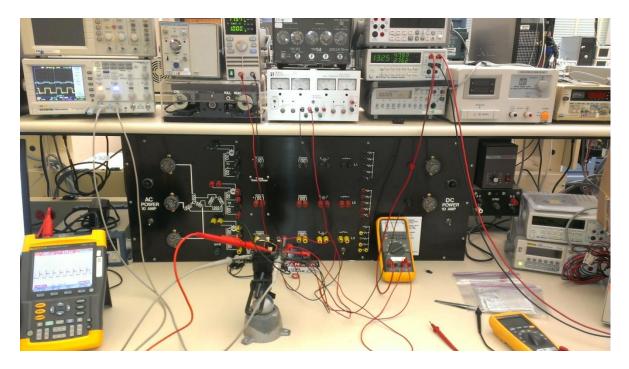


Figure 5-7: Test Set-up and Equipment Used for Testing Bi-directional DC-DC Converter 5.4. Bi-directional DC-DC Charging Flyback Hardware Results

The charging flyback must be able to supply a full load of 2A at a regulated voltage of 12.5V. Thus, the flyback will be tested in percent of load increments to monitor the efficiency of the flyback. Also, the output voltage ripple will be observed as well as the gate voltages of both flyback controllers to prove that while the charging flyback is commutating, the discharging flyback is disabled.

Table 5-1 shows the output voltages and efficiencies for the charging flyback ranging from 0.1A load to 2A full load. The output voltage slightly decreases as the output current increases. The drop in output voltage can be attributed to a combination of switch conduction losses and copper losses. Input power is calculated based upon the input voltage measured by the power meter and the input current measured by a digital multimeter. Output power is calculated based upon the output voltage measured by the digital multimeter and the output current displayed on the electronic load.

Input Voltage (V)	Input Current (A)	Output Voltage (V)	Output Current (A)	Input Power (W)	Output Power (W)	Efficiency (%)
48.00	0.083	12.20	0.20	4.0	2.4	61.24
48.00	0.142	12.39	0.40	6.8	5.0	72.71
48.00	0.195	12.28	0.60	9.4	7.4	78.72
48.00	0.249	12.31	0.80	12.0	9.8	82.40
48.00	0.306	12.32	1.00	14.7	12.3	83.79
48.00	0.356	12.10	1.20	17.1	14.5	84.97
48.00	0.409	11.98	1.40	19.6	16.8	85.37
48.00	0.472	12.15	1.60	22.7	19.4	85.75
48.00	0.521	11.95	1.80	25.0	21.5	85.96
48.00	0.576	11.88	2.00	27.6	23.7	85.89
46.00	0.6	11.94	2.00	27.6	23.9	86.52
50.00	0.55	11.97	2.00	27.5	24	87.05

Table 5-1: Output Voltages and Efficiencies for Percent Load Test of Charging Flyback

Load regulation was calculated using Equation 5.1 shown below:

Load Regulation (%) =
$$\left(\frac{12.2V - 11.88V}{11.88V}\right) * 100 = 2.6\%$$
 (5.1)

Line regulation was calculated using Equation 5.2 shown below:

Line Regulation (%) =
$$\left(\frac{11.97V - 11.94V}{11.88V}\right) * 100 = 0.252\%$$
 (5.2)

Efficiency was calculated using Equation 5.3 provided below:

$$\eta(\%) = \frac{P_{out}}{P_{in}} * 100\%$$
(5.3)

The load and line regulations for the charging flyback meet the requirement of less than 5%. Figure 5-8 shows a graph of the efficiency of the charging flyback of the bi-directional DC-DC converter over percentage of load. Compared to the design requirements stated in Chapter 3, the efficiency of the charging flyback is above 80% for all loads above 30% of the full load.

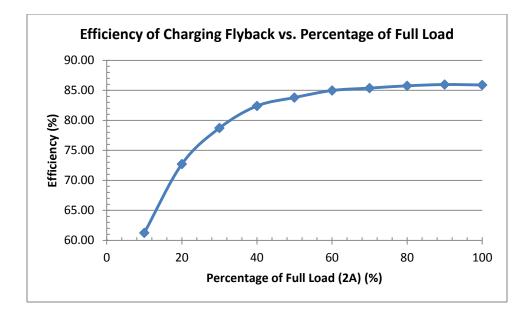


Figure 5-8: Efficiency vs. Percent Load for Charging Flyback

Figure 5-9 shows the gate voltage pin of the charging LT3748 controller chip and the switching voltage across the drain-to-source of the MOSFET at full load conditions. Figure 5-10 shows the sense voltage at the current sense pin of the LT3748 controller chip and the output voltage peak-to-peak ripple. As seen in the Figure 5-10, the voltage across the sense resistor drops to zero within each switching period, signifying that the flyback is running in boundary conduction mode. Since the inductor current goes to zero within a switching cycle, the voltage across the sense resistor will also reach zero within each switching period. The voltage across the sense resistor is within the voltage threshold of 100mV for the SENSE pin of the LT3748 chip.

Figure 5-11 shows the output voltage peak-to-peak ripple of the charging flyback at full load conditions. With a measured peak-to-peak voltage of 1.9V, the output voltage ripple can be calculated using Equation 5.4:

$$\% \frac{\Delta V}{V_o} = \frac{1.9V}{11.88V} * 100 = 16\%$$
(5.4)

Compared to the simulation results in Chapter 4, hardware results such as the efficiency, line regulation, load regulation, and output voltage of the charging flyback meet the

requirements. The peak-to-peak output voltage of the charging flyback at full load conditions is higher than the required 5% defined in Chapter 3. A smaller peak-to-peak ripple voltage can be achieved by adding additional capacitance at the output of the flyback.

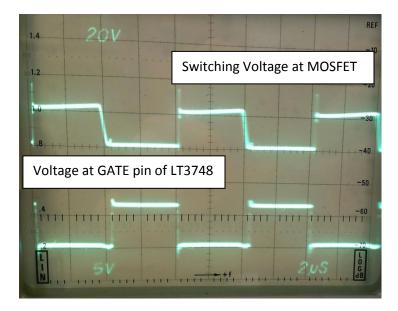


Figure 5-9: Gate Voltage for the Charging LT3748 Controller Chip and Switching Voltage across Switching MOSFET (Drain-to-Source) at Full Load Conditions

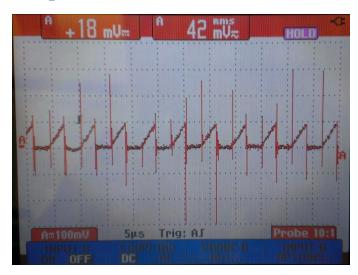


Figure 5-10: Current Sense Voltage of the Sense Resistor for the Charging Flyback and Output Voltage Peak-to-Peak Ripple at Full Load Conditions

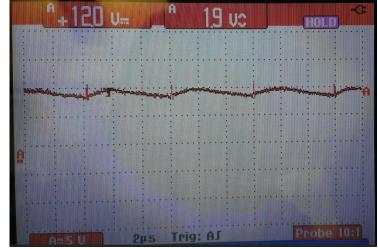


Figure 5-11: Output Voltage Peak-to-Peak Ripple of Charging Flyback at Full Load Conditions

5.5. Bi-directional DC-DC Discharging Flyback Hardware Results

The discharging flyback must be able to supply a full load of 1A at a regulated voltage of 48V. Thus, the discharging flyback will be tested in similar fashion as the charging flyback with percent of load increments to monitor the efficiency of the flyback. Also, the output voltage ripple will be observed as well as the gate voltages of both flyback controllers to prove that while the discharging flyback is commutating, the charging flyback is disabled.

Table 5-2 shows the output voltages and efficiencies for the discharging flyback ranging from 0.05A load to 0.7A load. The output voltage slightly decreases as the output current increases. The drop in output voltage can be attributed to a combination of switch conduction losses and copper losses. Input power is calculated based upon the input voltage measured by the power meter and the input current measured by a digital multimeter. Output power is calculated based upon the output voltage measured by the digital multimeter and the output current displayed on the electronic load.

Input Voltage (V)	Input Current (A)	Output Voltage (V)	Output Current (A)	Input Power (W)	Output Power (W)	Efficiency (%)
12	0.31	50.2	0.05	3.7	2.5	67.47
12	0.56	50.1	0.1	6.7	5.0	74.55
12	0.8	50	0.15	9.6	7.5	78.13
12	1.01	50	0.2	12.1	10.0	82.51
12	1.24	50	0.25	14.9	12.5	84.01
12	1.47	49.9	0.3	17.6	15.0	84.86
12	1.69	49.9	0.35	20.3	17.5	86.12
12	1.92	49.8	0.4	23.0	19.9	86.46
12	2.14	49.7	0.45	25.7	22.4	87.09
12	2.39	49.6	0.5	28.7	24.8	86.47
12	2.62	49.5	0.55	31.4	27.2	86.59
12	2.86	49.3	0.6	34.3	29.6	86.19
12	3.11	49.1	0.65	37.3	31.9	85.52
12	3.36	48.8	0.7	40.3	34.2	84.72
13	3.07	48.9	0.7	39.9	34.3	85.77
11	3.67	48	0.7	40.3	33.6	83.23

Table 5-2: Output Voltages and Efficiencies for Percent Load Test of Discharging Flyback

Load regulation was calculated using Equation 5.5 shown below:

Load Regulation (%) =
$$\left(\frac{50.2V - 48.8V}{48.8V}\right) * 100 = 2.87\%$$
 (5.5)

Line regulation was calculated using Equation 5.6 shown below:

Line Regulation (%) =
$$\left(\frac{11.97V - 11.94V}{11.93V}\right) * 100 = 1.84\%$$
 (5.6)

Efficiency was calculated using Equation 5.7 provided below:

$$\eta(\%) = \frac{P_{out}}{P_{in}} * 100\%$$
(5.7)

The load and line regulations for the discharging flyback meet the requirement of less than 5% defined in Chapter 3. Figure 5-11 shows a graph of the efficiency of the discharging flyback of the bi-directional DC-DC converter over percentage of load. Compared to the design requirements stated in Chapter 3, the efficiency of the charging flyback is above 80% for all loads above 25% of the full load.

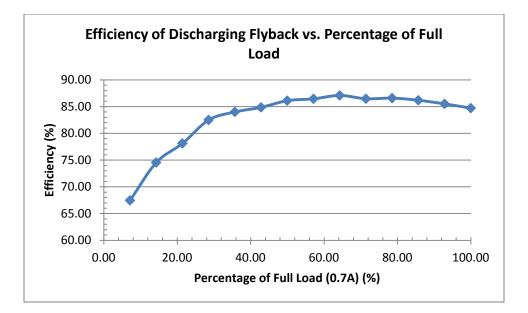


Figure 5-12: Efficiency vs. Percent Load for Discharging Flyback

Figure 5-13 shows the gate voltage pin of the discharging LT3748 controller chip and the switching voltage across the drain-to-source of the MOSFET at full load conditions. Figure 5-14 shows the sense voltage at the current sense pin of the LT3748 controller chip. As seen in Figure 5-14, the voltage across the sense resistor drops to zero within each switching period, signifying that the flyback is running in boundary conduction mode. Since the inductor current goes to zero within a switching cycle, the voltage across the sense resistor will also reach zero within each switching period. The voltage across the sense resistor is within the voltage threshold of 100mV for the SENSE pin of the LT3748 chip.

Figure 5-15 shows the output voltage peak-to-peak ripple of the discharging flyback at full load conditions. With a measured peak-to-peak voltage of 4V, the output voltage ripple can be calculated using Equation 5.4:

$$\% \frac{\Delta V}{V_o} = \frac{4V}{48.8V} * 100 = 8.2\%$$
(5.8)

Compared to the simulation results in Chapter 4, hardware results such as the efficiency, line regulation, load regulation, and output voltage of the discharging flyback meet the

requirements. The peak-to-peak output voltage of the discharging flyback at full load conditions is higher than the required 5% defined in Chapter 3. A smaller peak-to-peak ripple voltage can be achieved by adding additional capacitance at the output of the flyback.

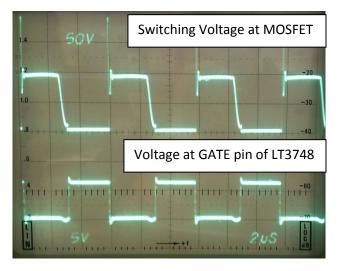


Figure 5-13: Gate Voltage for the Discharging LT3748 Controller Chip and Switching Voltage across Switching MOSFET (Drain-to-Source) at Full Load Conditions

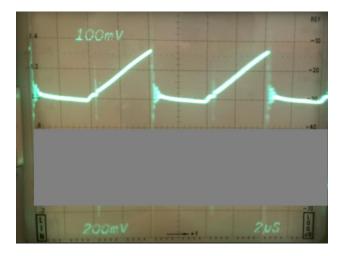


Figure 5-14: Current Sense Voltage for Discharging Flyback at Full Load Conditions

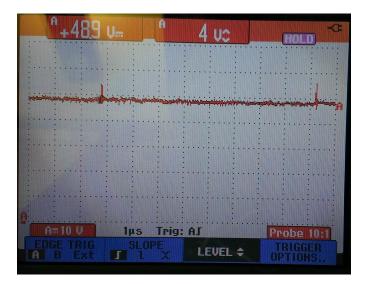


Figure 5-15: Output Voltage Peak-to-Peak Ripple of Charging Flyback at Full Load Conditions

Table 5-3 shows a summary of the hardware results and simulation results from Chapter 4 compared to the design requirements specified in Chapter 3. All electrical specifications are met except for the peak-to-peak output voltage ripple of each flyback. Although the application of the bi-directional DC-DC converter will not be greatly affected by a large peak-to-peak output voltage ripple, a smaller ripple can be achieved as stated earlier in this chapter by providing a larger capacitance at the output voltage with a low ESR to improve the overall efficiency of the system.

	Cha	rging Flybac	k	Discharging Flyback			
	Design Requirement	Simulation Results	Hardware Results	Design Requirement	Simulation Results	Hardware Results	
Input Voltage							
	48V	48V	48V	12V	12V	12V	
Output Voltage	12.5V	12.6V	11.88V	48V	48.3V	48.8V	
Full Load Current	2A	2A	2A	1A	1A	0.7A	
Full Load Output Wattage	25W	26.6W	24W	48W	53W	34W	
Line Regulation							
	5%	0%	0.25%	5%	0%	1.8%	
Load Regulation							
	5%	0.7%	2.6%	5%	0.2%	2.9%	
Output Voltage Ripple		-					
	5%	2.4%	16%	5%	0.3%	8.2%	
Efficiency at Full Load							
	$\geq 80\%$	95 %	86%	$\geq 80\%$	92%	85%	

Table 5-3: Design Requirements Summary after Simulation and Hardware Results

Chapter 6 – Conclusion and Future Improvement

The objective of this thesis was to investigate the use of the flyback topology for the bidirectional DC-DC power converter. The bi-directional power converter would be needed for the battery system used in the DC House project. The proposed system should be able to charge the battery from and to discharge the battery to the DC House 48 V system bus.

The bi-directional converter did meet most of the target electrical constraints stated in Chapter 3. During hardware implementation, the converter was able to provide a single path power flow for both the discharging and charging flyback using the LT1716 control scheme. For the charging flyback, the bi-directional converter was able to operate from an input voltage ranging from 11V to 13V at excellent line regulation. The charging flyback also produced an efficiency of 86% with a total output power of 24W at full load conditions of 2A. The charging flyback was also able to maintain load regulation from a minimum load of 0.2A up to a full load of 2A.

For the discharging flyback, the bi-directional converter was able to operate from an input voltage ranging from 46V to 50V at excellent line regulation. The discharging flyback also produced an efficiency of 85% with a total output power of 34W at full load conditions of 0.7A. The discharging flyback was also able to maintain load regulation from a minimum load of 0.05A up to a full load of 0.7A.

Some issues concerning the operation of the converter involved the cleanliness of the signal going into the current sense pins of both controller chips. A possible improvement may be to use a more effective RC filter to cutoff any unwanted noise to the pin in order for the controller chip to not falsely turn off. The custom transformer also affects the efficiency of the

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system since the ringing of the transformer creates losses during operation. An improved transformer design may help improve the efficiency of the bi-directional converter.

Although the concept of the bi-directional converter is feasible, further improvements can be done in the future such as a better control scheme, larger output power capability, and implementation of the converter with the DC House system. The current control scheme does allow the converter to switch between the discharging and charging flyback. However, the exchange between each flyback is centered on the set voltage of 11V. Thus, the charging and discharging flybacks can only operate between the battery voltages of 11V to 11.1V. An improved control scheme would allow the bi-directional converter to operate for a wider battery voltage range.

As stated in Chapter 3, the desired output power of the bi-directional converter is 150W based upon the charging and discharging time of the battery. Currently, the proposed bidirectional converter is able to supply 35W using the flyback topology. Using other topologies or improving on the flyback design of the converter can help achieve the ultimate goal of an output power of 150W. The final implementation of the converter with the DC House system is also necessary to see the discharging and charging times necessary for the battery with respect to the house. Protection schemes such as fuses or current limiting applications on the battery side are needed to preserve not only the battery but the 48V DC bus line that feeds into the DC House. Once the converter is added onto the DC House system, efficiency and load and line regulations should be investigated to see if the battery is a feasible backup power source.

Overall, this thesis successfully demonstrates the ability to use a single stage flyback converter to provide bi-directional charging/discharging of a battery system.

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Appendix A – Transformer Core Datasheet

The following information is specification data for transformer ferrite core PQ35/35:

Ferroxcube

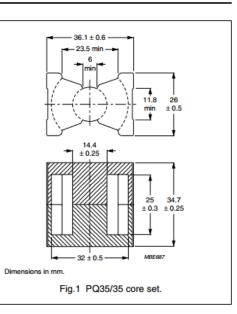
PQ cores and accessories

PQ35/35

CORE SETS

Effective core parameters

SYMBOL	PARAMETER	VALUE	UNIT
Σ(I/A)	core factor (C1)	0.454	mm ⁻¹
Ve	effective volume	16300	mm ³
le	effective length	86.1	mm
Ae	effective area	190	mm ²
A _{min}	minimum area	162	mm ²
m	mass of set	= 73	g



PQ cores and accessories

PQ35/35

GRADE	A _L (nH)	μ _e	TOTAL AIR GAP (μm)	TYPE NUMBER
3F3	315 ±3%	≈ 114	<i>≈</i> 920	PQ35/35-3F3-E315
	400 ±3%	≈ 144	≈ 690	PQ35/35-3F3-E400
	630 ±3%	≈ 227	≈ 400	PQ35/35-3F3-A630
	1000 ±3%	≈ 361	≈ 230	PQ35/35-3F3-A1000
	1600 ±5%	≈ 577	≈ 120	PQ35/35-3F3-A1600
	4570 ±25%	≈ 1650	= 0	PQ35/35-3F3

Properties of core sets under power conditions

	B (mT) at		CORE LOSS (W) at					
GRADE	H = 250 A/m; f = 25 kHz; T = 100 °C	f = 25 kHz; B = 200 mT; T = 100 °C	f = 100 kHz;	f = 100 kHz; B = 200 mT; T = 25 °C	f = 100 kHz; B = 200 mT; T = 100 °C	f = 400 kHz; B = 50 mT; T = 100 °C	f = 500 kHz; B = 50 mT; T = 100 °C	
3C81	≥320	≤ 3.8	-	-	-	-	-	
3C90	≥320	≤ 2.0	≤2.1	-	-	-	-	
3C91	≥320	-	≤ 1.2 ⁽¹⁾	-	≤ 8.0 ⁽¹⁾	-	-	
3C94	≥320	-	≤ 1.6	-	≤ 10	-	-	
3C95	≥320	-	-	≤ 10.3	≤ 9.78	-	-	
3C96	≥340	-	≤ 1.2	-	≤ 8.0	≤ 3.0	≤ 6.1	
3F3	≥320	-	≤ 1.8	-	-	≤ 3.1	-	

Note

1. Measured at 60 °C.